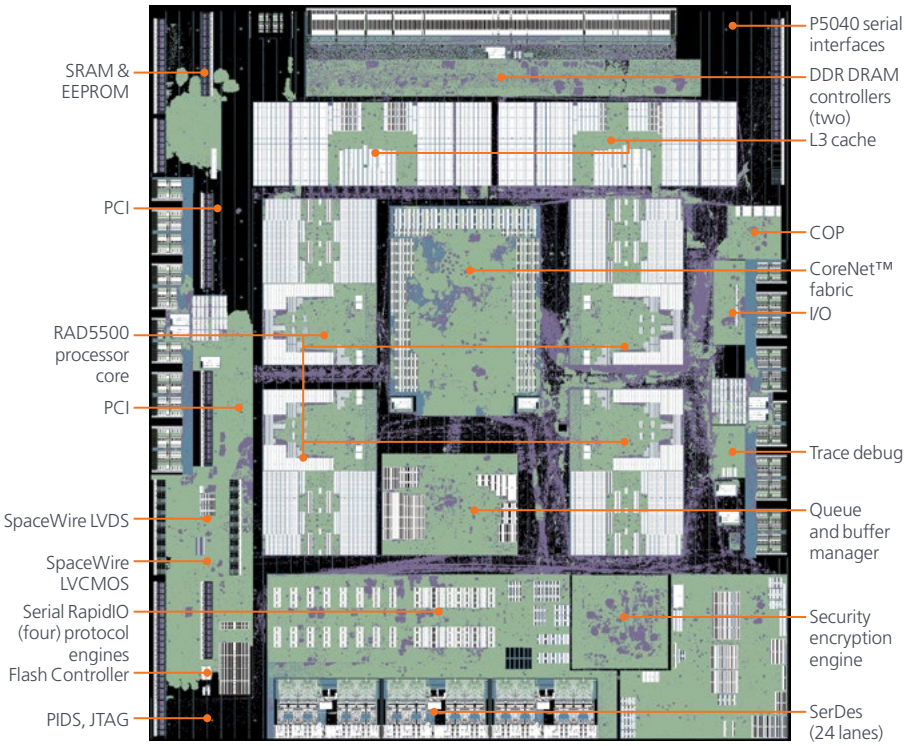
BAE SYSTEMS
INSPIRED WORK

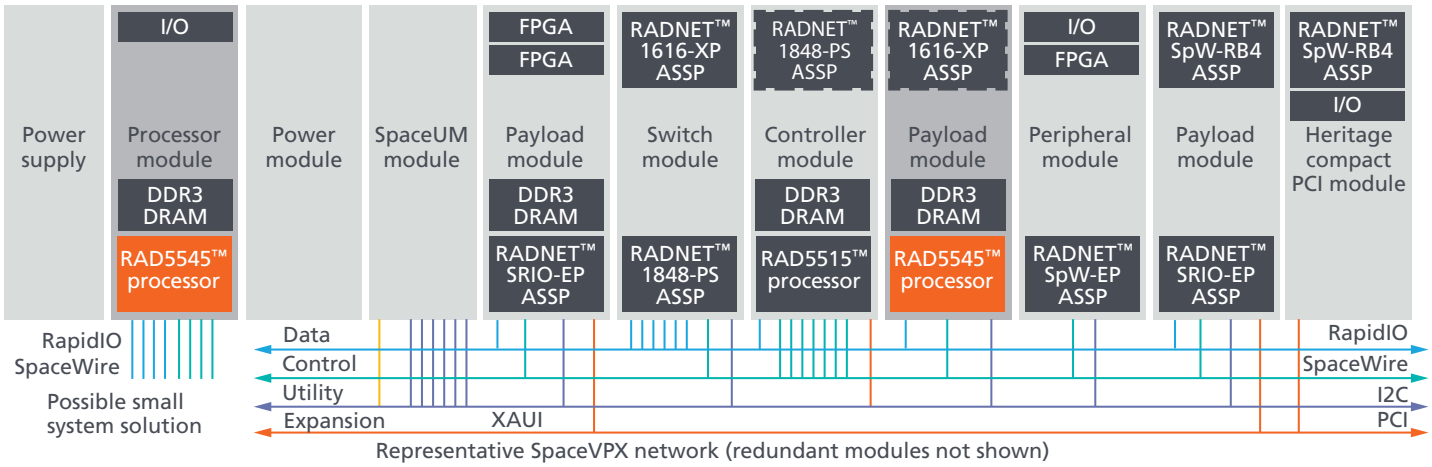
RAD5545™ multi-core system-on-chip Power Architecture® processor

The RAD5545 multi-core processor is a highly integrated solution with an order of magnitude leap in performance for emerging on-board processing applications.

The RAD5545 system-on-chip (SoC) microprocessor offers a balanced combination of three capabilities – Power Architecture processors for portability of heritage software, large memory capacity powered by dual interleaved DDR2/3 DRAM memory interfaces, and high I/O throughput based on serializer/deserializer (SerDes) high-speed links.

The RAD5545 SoC microprocessor singlehandedly replaces multiple cards of previous generations with four RAD5500™ 32/64-bit Power Architecture processor cores, three levels of on-die cache, four RapidIO® (SRIO) ports, and a 16-port SpaceWire router.





Representative SpaceVPX network (redundant modules not shown)

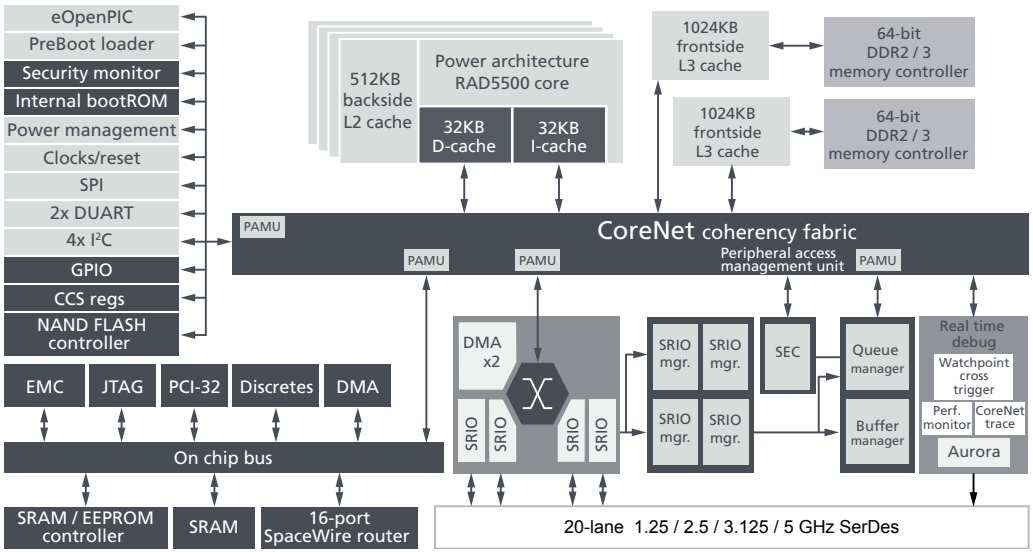
Key features and benefits

- Reduced size, weight, and power based on the QorIQ® architecture enables support of various applications
- Processor throughput of up to 5.6 giga operations per second (GOPS)/ 3.7 GFLOPS and memory bandwidth of up to 102 Gb/s and I/O throughput of up to 64 Gb/s enables superior efficiency
- Designed for insertion into the SpaceVPX standard, supporting the RapidIO data plane, SpaceWire control plane, and inter-integrated circuit (I2C) utility plane
- 16-port router supports space-specific SpaceWire serial protocol
- 64-bit core increases performance, supporting direct addressability to 64GB of memory, improving double precision floating point performance, and achieving 3.0 Dhrystone MIPS (DMIPS)/MHz
- Multiple levels of cache memory minimizes access to main memory, maximizing effective throughput
- Trust architecture infrastructure provides secure boot, integrity code testing, data encryption, and partitioning of the system to prevent unauthorized access to memory locations, enabling secure operation
- 32-bit parallel peripheral component interconnects (PCI) interface enables legacy connections
- Four serial RapidIO ports implement efficient handling of RapidIO message and streaming data packets
- Data Path Acceleration Architecture (DPAA) offloads functions from processor cores to further their effectiveness

Specifications

Technology	Radiation-hardened by design RH45® circuit library
	Trusted foundry 45nm silicon-on-insulator (SOI) process
	1752-pin, 45mm ceramic column grid array package
Temperature	Operating at -55 to +125 degrees Celsius
Radiation-hardness	Total ionizing dose: 1 Mrad (Si)
	Single event upset (SEU): SRAMs: <2E-9 upsets/ bit-day, prior to the integrated ECC correction
	SEU: Flip-flops: 8E-14 upsets/bit-day
	Latch-up immune
Power Supply	0.95 V +/- 5 percent core
	1.5 or 1.8 V +/- 5 percent SerDes and double data rate (DDR) I/O
	1.8 V, 2.5 V, and/or 3.3 V I/O (user programmable)
Power dissipation	17.7 watts at 95 degrees Celsius and +5 percent voltage
	All interfaces operational
Interfaces	
Input and output	Four serial RapidIO ports across 16 lanes; up to 5 Gbaud/lane
	16 SpaceWire links with embedded router
	Four I2C interfaces
	Serial peripheral interface (SPI)
	32-bit parallel PCI
	Two dual UARTs (four simple or two advanced)
Memory	Dual DDR2/3 DRAM interfaces with interleaving
	NAND flash controller
	SRAM/EEPROM controller
Test and debug	Aurora protocol SerDes trace/debug
	JTAG master and slave interfaces

Hardware block diagram



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BUILT ON Power