

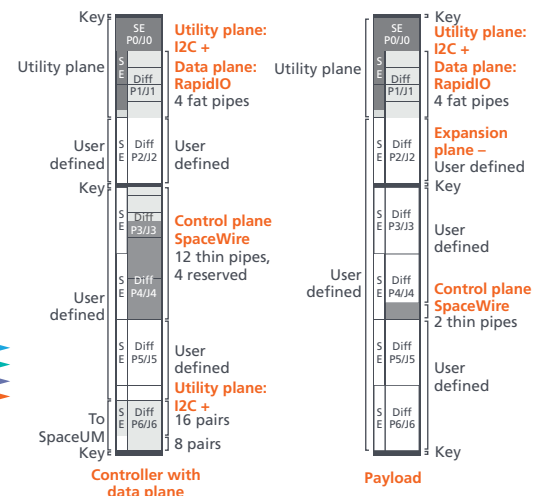
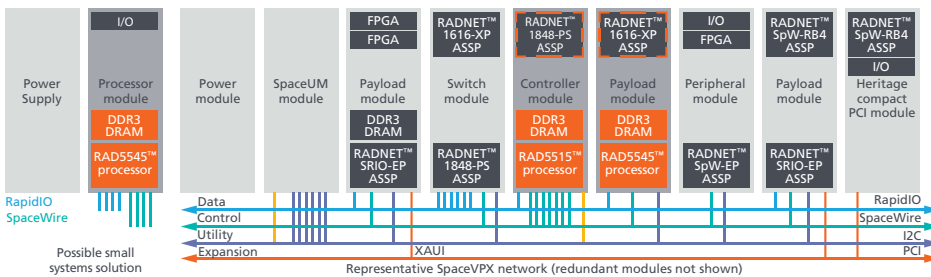
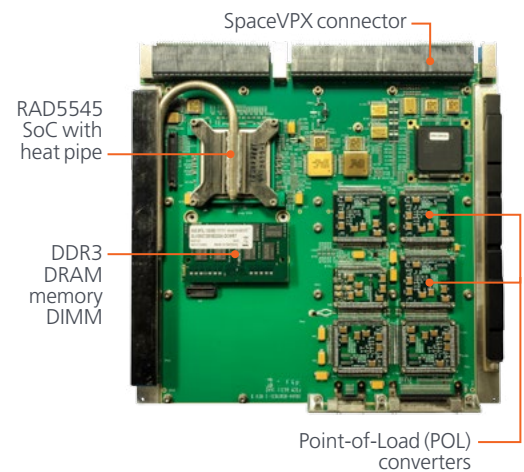
# RAD5545™ SpaceVPX single-board computer

Multi-core single-board computer

The RAD5545™ SpaceVPX single-board computer (SBC) integrates either the RAD5515™ or RAD5545 system-on-chip (SoC) processor with volatile and non-volatile memory on a 6U-220 format module compliant to the ANSI/VITA 78.00 SpaceVPX standard.

The SBC is designed to support operation as either a payload or system controller in a SpaceVPX backplane. Based on BAE Systems' RAD5545 or RAD5515 QorIQ® Power Architecture® radiation-hardened SoC processor, the SBC offers both high performance and high I/O throughput.

It includes up to 16 GBytes of DDR3 SDRAM with error correction at 800 MTransfers/second and up to 8 GBytes of triple modular redundant non-volatile flash memory. Up to four RapidIO ports at 16 Gbits/second each and 12 SpaceWire links at 320 Mbits/second each are provided to the SpaceVPX backplane. An optional daughter card with PCI, RapidIO, and/or SpaceWire interfaces can be used to personalize the SBC for unique needs.



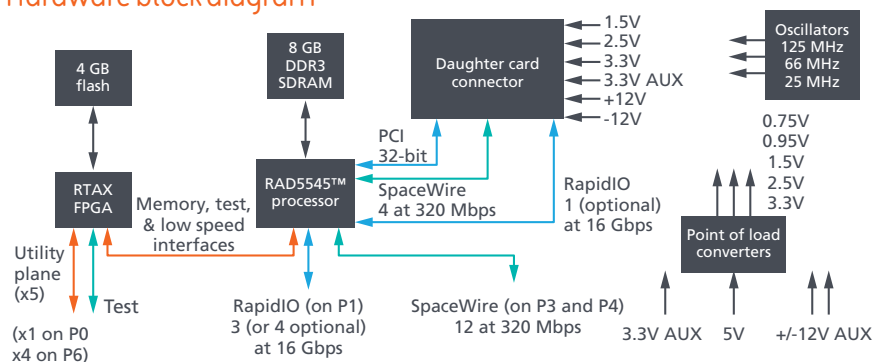
## Key features and benefits

- Processor throughput of up to 5.6 giga-operations per second/3.7 giga-floating-point operations per second offers more than 10 times the performance of the fastest RAD750® processor
- Memory bandwidth of up to 51 Gb/s and I/O throughput of up to 64 Gb/s provide balance to prevent bottlenecks to or from the processor cores
- Dual in-line memory module mounting supports ease of memory replacement or upgrade
- Optional user-personalized daughter card with parallel peripheral component interconnect, RapidIO, and/or SpaceWire interfaces supports mission-specific SBC personalization
- Designed for insertion into the SpaceVPX backplane, supporting the RapidIO data plane, SpaceWire control plane, and system management inter-integrated circuit utility plane for interoperability with other SpaceVPX-compliant boards
- Multiple levels of on-die cache and high-performance DDR3 main memory all with error correction provide maximum effective throughput and reliability
- Triple modular redundant (TMR) flash memory enables high-density, non-volatile storage with high reliability
- Trust architecture security infrastructure provides secure boot, integrity code testing, data encryption, and partitioning of the system to minimize the likelihood of corruption due to intentional or environmental-based intrusion
- Up to four RapidIO ports with integrated message managers support high-performance data streaming and messaging and support system architectures based on either mesh or switch-based backplanes

## Specifications

|                                 |   |
|---------------------------------|---|
| <b>SpaceVPX</b>                 | Slot profiles: payload, system controller with data plane<br>Module profiles:<br>Payload: MOD6-PAY-4F1Q2T-12.2.1-5-22<br>Controller: MOD6-CON-4F12T12U-12.6.1-2-22  |
|                                 | Mechanical size: 6U-220   |
|                                 | Card pitch: 1.2 inches  |
|                                 | Cooling: Conduction   |
|                                 | Power profile (no daughter card)<br>5.0 V (+/- 10 percent): 6.7 Amps<br>3.3 V AUX: <1.0 Amps  |
|                                 | User-defined I/O: Differential  |
| <b>Temperature</b>              | Operating at -55 to +125 degrees Celsius  |
| <b>Radiation-hardness</b>       | Total ionizing dose: 100 Krad (Si)<br>Single event upset: 1e-3 upsets/card-day<br>Latchup immune  |
| <b>Power dissipation</b>        | 35 Watts at 95 degrees Celsius and +5 percent voltage with all dissipation interfaces operational (no daughter card)  |
| <b>Interfaces</b>               | Up to four 4-lane RapidIO ports up to 5 Gbaud/lane (also supports 3.125, 2.5, and 1.25 Gbaud/lane)<br>Up to 12 SpaceWire serial links to the backplane up to 320 Mb/s each<br>I2C and related utility plane control signals<br>JTAG test and debug<br>Aurora high speed trace debug |
| <b>Daughter card interfaces</b> | Up to 4 SpaceWire links<br>One RapidIO port (the RapidIO port is mutually exclusive with the 4th RapidIO port to the backplane)<br>32-bit parallel PCI  |

## Hardware block diagram



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