The RADNET SRIO-EP application specific standard product (ASSP) provides connection between the RapidIO Revision 2.1 fabric and alternative interfaces along with access to large capacity DRAM memory.

The RADNET SRIO-EP ASSP is a member of BAE Systems’ RADNET family of high-performance radiation-hardened networking products. The ASSP integrates RapidIO and XAUI high-performance serial link interfaces with lower bandwidth legacy protocol interfaces. It is an extremely flexible general purpose connection device, which is compatible with the SpaceVPX standard.
Key features and benefits

- RapidIO interface operates up to 3.125 Gbaud per lane
- SpaceWire and inter-integrated circuit (I2C) interfaces for SpaceVPX control and utility planes
- Legacy interfaces include peripheral component interconnect (PCI) and MIL-STD-1553
- SpaceWire serial links supported by a four-port router
- Dual interleaved DDR2/3 DRAM controllers, a NAND flash controller, and an EEPROM controller
- 256KB of on-die SRAM for use by the on-die microcontrollers
- Pseudo-random binary sequence (PRBS) generation and detection is provided to allow bit error rate testing across the serializer/deserializer (SerDes) links
- Five embedded microcontrollers to support bridging and priority queuing capabilities
- Four serial RapidIO embedded microcontrollers support multiple interfaces and are capable of 64 Dhrystone MIPS (DMIPS) of processing
- Serial RapidIO embedded microcontrollers create and direct messages between interfaces using a built-in 4KB priority scoreboard for queue management
- Fifth user-programmable embedded microcontroller provides 27 DMIPS of fixed-point processing for ASSP command and data handling
- Embedded microcontrollers optimize support for extensive priority queue management
- Two XAUI interfaces provide high throughput user interfaces
- SelectMAP interface provides support to configure multiple Xilinx® FPGAs
- SerDes interfaces support the RapidIO short and long run specifications, with programmable pre- and post-emphasis drive levels
- Unused ports can be powered down

Specifications

| Technology | Radiation-hardened by design RH45® circuit library |
| Radiation-hardness | Total ionizing dose: 1 Mrad (Si) |
| | Single event upset (SEU): SRAMs: <2E-9 upsets/bit-day, prior to the integrated ECC correction |
| | SEU: Flip-flops: 8E-14 upsets/bit-day |
| | Latch-up immune |
| Power supply | 0.95 V +/- 5 percent core |
| | 1.5 or 1.8 V +/- 5 percent SerDes and double data rate (DDR) I/O |
| | 2.5 V low voltage differential signaling (LVDS) I/O |
| | 3.3 V CMOS I/O |
| Power dissipation | 4-11 watts at 95 degrees Celsius and +5 percent voltage; depends on combination of active interfaces |
| | Unused interfaces can be powered down |
| Interfaces | Dual interleaved DDR2/3 DRAM interfaces |
| | NAND flash controller |
| | EEPROM controller |
| Input/output | One four-lane Serial RapidIO port with redundant SerDes; up to 3.125 Gbaud/lane |
| | Two XAUI 802.3 four-lane ports (article 47 and 48 compliant) with redundant SerDes |
| | Four-port SpaceWire router |
| | Four I2C master/slave interfaces |
| | Serial peripheral interface (SPI) with four chip selects |
| | 36 discretes with clocks and timers |
| | 32-bit, 33 MHz PCI bus |
| | MIL-STD-1553B with A/B transceiver |
| | SelectMAP FPGA configuration interface |
| Test and debug | Dual JTAG master interface |

Hardware block diagram