**RADNET™ SpW-EP radiation-hardened SpaceWire endpoint ASSP**

The RADNET SpW-EP application specific standard product (ASSP) provides a low-power, high-performance connection between SpaceWire fabric, remote instruments and peripherals through a variety of matched interfaces.

The RADNET SpW-EP ASSP is a member of the RADNET family of high-performance radiation-hardened networking products, offering a simplified and dependable entry point to adopt the SpaceWire protocol with enhanced addressable network management features and high radiation resistance.

![RADNET SpW-EP ASSP Diagram](image-url)

- **Data**
- **Control**
- **Utility**
- **Expansion**
- **Representative SpaceVPX network (redundant modules not shown)**

**Key Components:**
- **FPGA**
- **DDR3 DRAM**
- **RADNET™ SRIO-EP ASSP**
- **I/O**
- **Heritage compact PCI module**

**Other Notable Components:**
- **SpaceWire router interface (RIF) with RMAP**
- **SpaceWire router/links**
- **SRAMs (two 16KB with ECC)**
- **FIFOs**
- **UART**
- **Embedded microcontroller**
- **Discretes**
- **12C**
- **SRIO-EP ASSP**
- **RADNET™ 1848-PS ASSP**
- **RADNET™ 1616-XP ASSP**
- **RAD5515™ processor**
- **RAD5545™ processor**

**Module Layout:**
- **Power module**
- **Space module**
- **Switch module**
- **Controller module**
- **Payload module**
- **Peripheral module**
- **I/O module**

**Connectors:**
- **RapidIO**
- **SpaceWire**
- **I2C**
- **PCI**

For more information, visit baesystems.com.
Key features and benefits

- Embedded controller provides support for protocol extensions and remote processing
- SpaceWire high-speed point-to-point serial link with low voltage differential signaling (LVDS) interfaces and remote memory access protocol (RMAP) support
- SpaceWire link data rates are supported up to 320 MHz, typically yielding 256 Mb/s per link
- 32 KB block of embedded SRAM is protected with ECC and provided for code or data storage
- 32-bit single bit error correction/double bit error detection (SEC/DED), error-protected external memory interface is available
- Four 32-bit up/down timers that are clocked and triggered internally or externally
- One internal 32-bit watchdog timer and SpaceWire TIC In/Out and time code support
- Phase-locked loop and various divisors
- RMAP function is supported and leveraged by newly available SpaceWire middleware for network discovery and management
- Integrated LVDS physical-layer circuits are cold sparsable, requiring no additional external components
- 32-bit RISC architecture embedded microcontroller enables users to autonomously manage SpaceWire or the auxiliary JTAG, FIFO, UART, 8- or 16-bit SelectMAP, serial peripheral interface (SPI), and inter-integrated circuit (I2C) interfaces
- External interface supports the use of either SRAM, PROM, or non-volatile Chalcogenide RAM

Specifications

<table>
<thead>
<tr>
<th>Technology</th>
<th>Radiation-hardened by design RH15™ circuit library</th>
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<tbody>
<tr>
<td></td>
<td>Trusted foundry 150 nm CMOS process</td>
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<tr>
<td></td>
<td>360-pin, 25mm ceramic column grid array</td>
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<td></td>
<td>180-340-pin ceramic quad flat pack (future)</td>
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<tr>
<td>Temperature</td>
<td>Operating at -55 to +125 degrees Celsius</td>
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<tr>
<td>Radiation-hardness</td>
<td>Total ionizing dose: 1 Mrad (Si)</td>
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<td></td>
<td>Single event upset (SEU): &lt;1E-10 upsets/bit-day</td>
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<tr>
<td></td>
<td>Latch-up immune</td>
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<tr>
<td>Power Supply</td>
<td>1.5 V +/- 5 percent core</td>
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<tr>
<td></td>
<td>3.3 V PCI, +/-10 percent I/O</td>
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<tr>
<td>Power dissipation</td>
<td>0.1 to 1.4 watts typical, depends on combination of active interfaces</td>
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<tr>
<td></td>
<td>1.4A maximum operational current</td>
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<tr>
<td>Interfaces</td>
<td>Memory 2GB SRAM/PROM interface with selectable parity or SEC/DED error connecting code</td>
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<tr>
<td>Input/output</td>
<td>One external SpaceWire port with dual LVDS physical layer (PHY); up to 320 Mbaud/lanes</td>
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<td>Port supports DMA-controlled RMAP access to the internal registers and memory</td>
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<td>32 discretes with clocks and timers</td>
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<td>32-bit bi-directional FIFO interface</td>
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<td></td>
<td>16-bit SelectMAP FPGA interface</td>
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<td></td>
<td>Dual I2C interfaces</td>
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<td>Serial peripheral interface (SPI)</td>
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<td>16550 UART interface</td>
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<tr>
<td>Test and debug</td>
<td>JTAG master and slave interfaces</td>
</tr>
</tbody>
</table>

Hardware block diagram

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