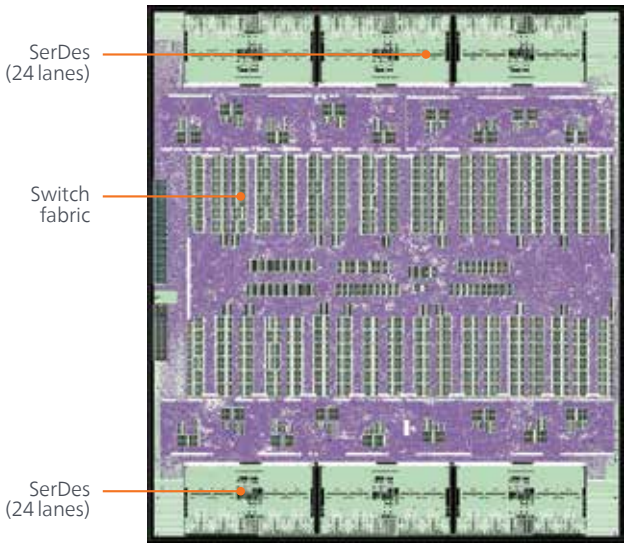
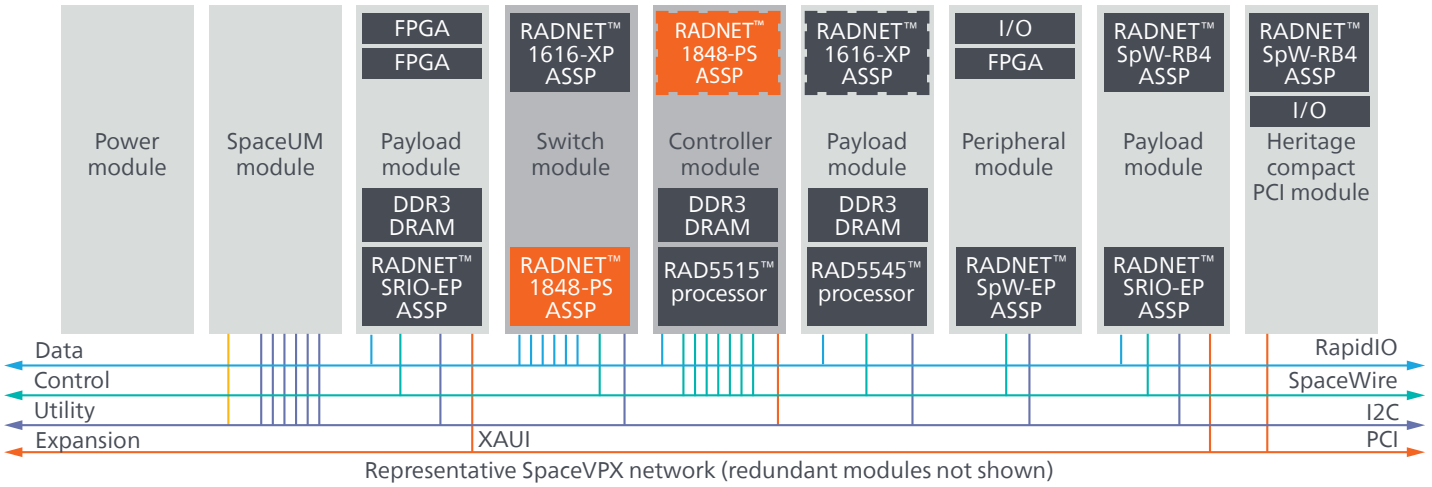
BAE SYSTEMS

RADNET™ 1848-PS radiation-hardened serial RapidIO® packet switch ASSP

The RADNET 1848-PS application specific standard product (ASSP) provides high-performance serial RapidIO revision 2.1 packet switching of up to 18 ports, enabling larger on-board RapidIO networks.

The RADNET 1848-PS ASSP is a member of the RADNET family of high-performance radiation-hardened networking products. Based on the industry-leading CPS-1848™ switch product licensed from Integrated Device Technology (IDT), the RADNET 1848-PS ASSP is a state-of-the-art switch that is compliant with the RapidIO revision 2.1 specification. It uses user-programmable ports of flexible width, allowing support for up to 12 four-lane (4x) ports, or up to 18 ports of varied widths (combinations of 1x, 2x, and 4x).





Representative SpaceVPX network (redundant modules not shown)

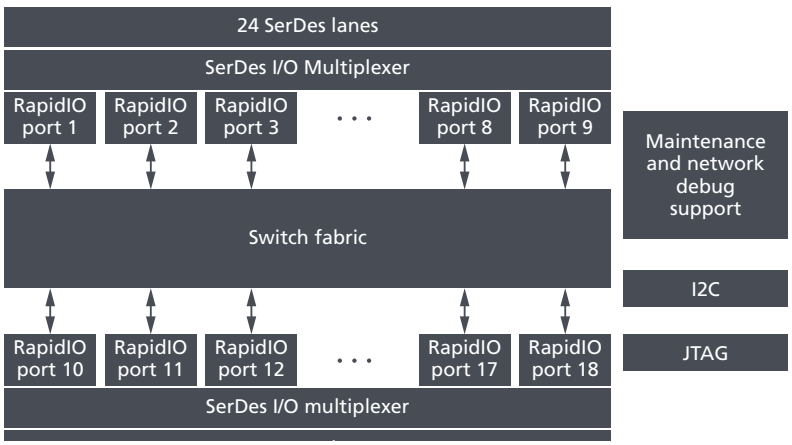
Key features and benefits

- Backwards compatible with RapidIO revision 1.3 components
- Provides a non-blocking crossbar packet switch with ports mapped across 48 lanes of serializer/deserializer (SerDes) circuitry at up to 3.125 Gbaud/lane rates
- Supports a full bandwidth of up to 120 Gb/s on up to 18 logical ports
- SerDes interfaces support the RapidIO short and long run specifications, with programmable pre- and post-emphasis and drive levels
- Pseudo-random binary sequence (PRBS) generation and detection to allow bit error rate testing across the SerDes links
- Supports both transmitter and receiver-based RapidIO flow control along with critical request flow (CRF) priority
- Powerful multicast support is incorporated with up to 40 multicast groups per port
- Switch ASSP is designed for insertion into SpaceVPX standard switch modules, supporting the RapidIO data plane and I2C utility plane
- Unused ports can be powered down for efficiency
- Ports can be individually reset to minimize network interruptions
- Provides strong support of the error management extensions
- Switch supports both store and forward and cut-through modes with minimized latency
- Inter-integrated circuit (I2C) master/slave interface is provided along with JTAG test and debug capability, allowing for configuration in any interface

Specifications

Technology	Radiation-hardened by design RH45® circuit library
	Trusted foundry 45nm silicon-on-insulator (SOI) process
	728-pin, 35mm ceramic column grid array package
Temperature	Operating at -55 to +125 degrees Celsius
Radiation-hardness	Total ionizing dose: 1 Mrad (Si)
	Single event upset (SEU): SRAMs: <2E-9 upsets/bit-day, prior to the integrated ECC correction
	Latch-up immune
Power Supply	0.95 V +/- 5 percent core
	1.5 V or 1.8 V +/- 5 percent SerDes I/O
	3.3 V PCI, +/-10 percent I/O
Power dissipation	14 watts at 95 degrees Celsius and +5 percent voltage with 12 four-lane ports operating at 3.125 Gbaud/lane
	Unused lanes/ports can be powered down
Composite throughput	120 Gb/s non-blocking bandwidth
Interfaces	
Input/output	Up to 18 serial RapidIO ports across 48 lanes; up to 3.125 Gbaud/lane
	I2C master/slave interface up to 1 Mbaud
Test and debug	JTAG slave interface

Hardware block diagram



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