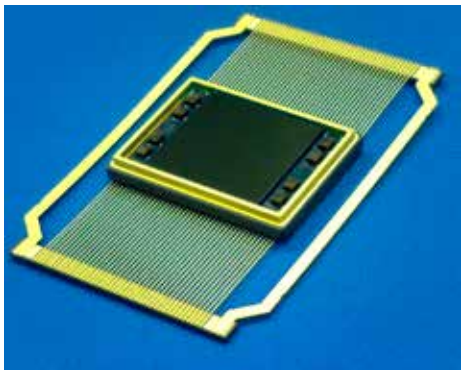
BAE SYSTEMS

Monolithic 512Mb radiation-hardened DDR3L SSRAM



Ultra-high-speed memory product

The monolithic 512Mb static random-access memory (SRAM) emulating double data rate third generation low voltage (DDR3L) synchronous dynamic random-access memory (SDRAM) operation is BAE Systems' next generation, ultra-high-speed memory product for users in the space community.

Capable of withstanding the effects of natural space and an upper radiation hardened environment, the monolithic 512Mb SRAM emulating DDR3L SDRAM operation has a total-dose tolerance of greater than 300Krad and an upset rate of less than 1E-12 upsets per bit-day.

Key features

- Transfer rate of 800 MT/s
- Operating frequency of 400 MHz
- Operating temperature range -55 °C to 125 °C
- Operating voltage (core) of 0.80 V
- Operating voltage (I/O) of 1.35 V
- Standby power < 40 mW typical, < 405 mW worst case
- Operating power < 125 mW typical
- Packaging 155-pin Ceramic Column Grid Array (CCGA)
- Synchronous operation
- Prototype and flight flows
- Latchup immune

System definitions

BA: 0-2 Bank address pins that select a particular bank in the memory during an ACTIVE, PRECHARGE, READ or WRITE command and define which mode register is loaded during the MODE REGISTER SET command.

A: 0-12 Address pins provide the row address for ACTIVATE commands, and the column address and auto precharge bit (10) for READ/WRITE commands, to select one location out of the memory array in a respective bank.

CS_L: Negative chip select at a low level enables the command decoder and at a high level masks all commands.

RAS_L, CAS_L, WE_L: Command inputs to the command decoder used to specify the various commands.

DQ: 0-7 Bi-directional data pins that serve as data outputs during a READ command and as data inputs during a WRITE command.

DQS_P, DQS_N: Bi-directional data strobe that are edge-aligned output with read data and center-aligned input with write data.

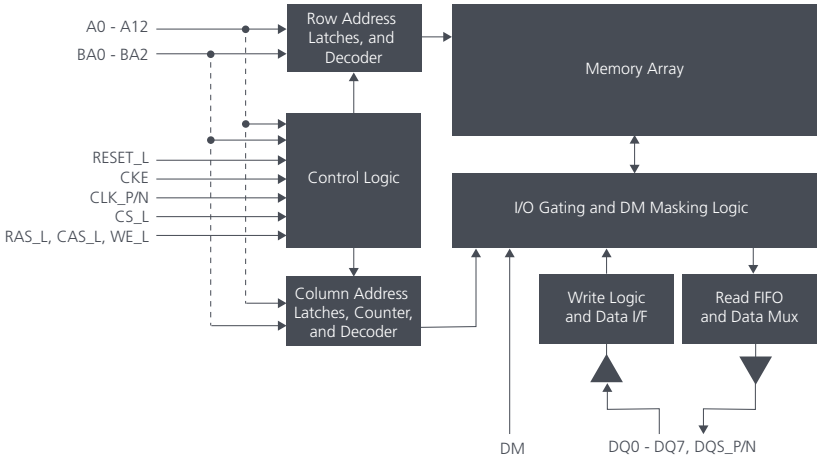
DM: Data mask input for write data during a WRITE command.

CLK_P, CLK_N: Differential clock inputs that sample all control and address input signals upon the crossing of the positive edge of CLK_P and the negative edge of CLK_N.

CKE: Clock enable input at a high level enables internal circuitry and clocks.

RESET_L: Asynchronous reset signal at a low level will reset and initialize the internal state machine and registers.

SEL_PRECH_ENA: Selective precharge enable at a high level will enable the precharge function.



Specifications

512 Mb SRAM emulating DDR3L SDRAM operation family of products	512 Mb single-chip (monolithic), up to 1Gb multi-chip module (MCM) available – 64M x 8 (monolithic) – 128M x 8 (MCM)

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