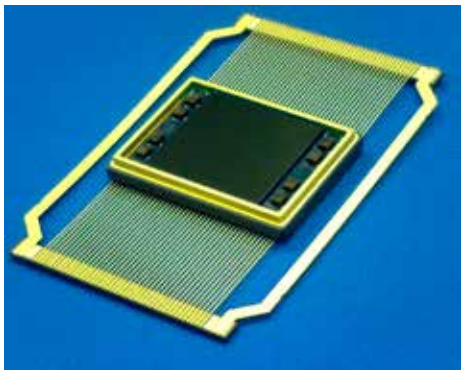
BAE SYSTEMS

Monolithic 64Mb radiation-hardened SDR SSRAM



High-speed memory product

The monolithic 64Mb static random-access memory (SRAM) emulating single data rate (SDR) synchronous dynamic random-access memory (SDRAM) operation is BAE Systems' next generation, high-speed memory product for users in the space community.

Capable of withstanding the effects of natural space and an upper radiation hardened environment, the monolithic 64Mb SRAM emulating SDRAM operation has a total-dose tolerance of greater than 300Krad and an upset rate of less than 1E-08 upsets per bit-day.

Key features

- Read/write access times of 5.4 nS
- Operating frequency 133.33 MHz
- Operating temperature range -55 °C to 125 °C
- Operating voltage (core) 0.8 V
- Operating voltage (I/O) 1.8 V
- Standby power < 8 mW typical, < 265 mW worst case
- Operating power < 15 mW/MHz typical
- Packaging organic multilayer flip-chip ball grid array
- Synchronous operation
- Prototype and flight flows
- Latchup immune

System definitions

BA:0-1 Bank address pins that select a particular bank in the memory during an ACTIVE, PRECHARGE, READ or WRITE command.

A: 0-11 Address pins that select a particular row during an ACTIVE command (0-11) and a particular column during the READ or WRITE commands (0-9).

CS_L: Negative chip select at a low level indicates that the SDRAM chip is selected for the current operation.

WE_L: Negative write enable at a low level indicates a WRITE command to the selected address.

RAS_L: Input to the command decoder used to specify the various commands.

CAS_L: Input to the command decoder used to specify the various commands.

DQ: 0-3 Bi-directional data pins that serve as data outputs during a READ command and as data inputs during a WRITE command.

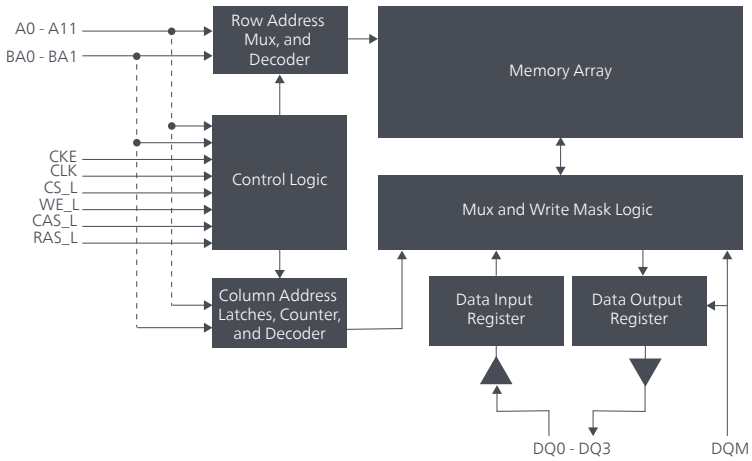
DQM: Data mask at a high level indicates the input data on DQ shall be masked from being written to the internal memory during a WRITE command and will tri-state DQ pins during a READ command.

CLK: Clock signal by which all operations will occur on the rising edge.

CKE: Clock enable at a low level will gate the internal clock one cycle later and at a high level will generate the internal clock one cycle later.

RESET_L: Asynchronous reset signal at a low level will reset and initialize the internal state machine and registers.

SEL_PRECH_ENA: Selective precharge enable at a high level will enable the precharge function.



Specifications

64Mb SRAM emulating SDRAM operation family of products	64Mb single-chip (monolithic), up to 256Mb multi-chip module (MCM) available – 16M x 4 (monolithic) – 16M x 16 (MCM)

For more information contact:

BAE Systems
Michael Marasciula
9300 Wellington Road
Manassas, Virginia 20110-4122
E: michael.marasciula@baesystems.us
W: baesystems.com/space

Cleared for open publication on 5/23.