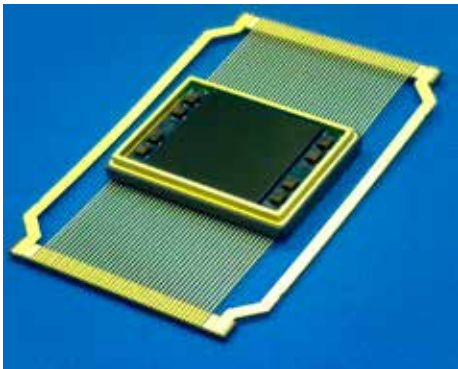


# Monolithic 80M radiation-hardened SRAM



## High-density memory product

The monolithic 80 Mb static random access memory is BAE Systems' next generation, high-density memory product for users in the space community.

## Description

Capable of withstanding the effects of natural space and an upper radiation hardened environment, the 80 Mb monolithic SRAM has a total-dose tolerance of greater than 300Krad and an upset rate of less than 1E-09 upsets per bit-day.

## Key features

- Read/write access times  $\leq 20\text{nS}$
- Operating temperature range  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$
- Operating voltage (core) 1.0V
- Operating voltage (I/O) 1.8V
- Standby power  $< 30\text{ mW}$  typical,  $< 350\text{ mW}$  worst case
- Operating power  $< 5\text{ mW/MHz}$  typical
- Packaging 96-lead ceramic flatpack
- Asynchronous operation
- Prototype and flight flows
- Latchup-immune

## System definitions

**A:** 0-22 (MCM) or 0-20 (SCM) address input pins that select a particular data entry within the memory array.

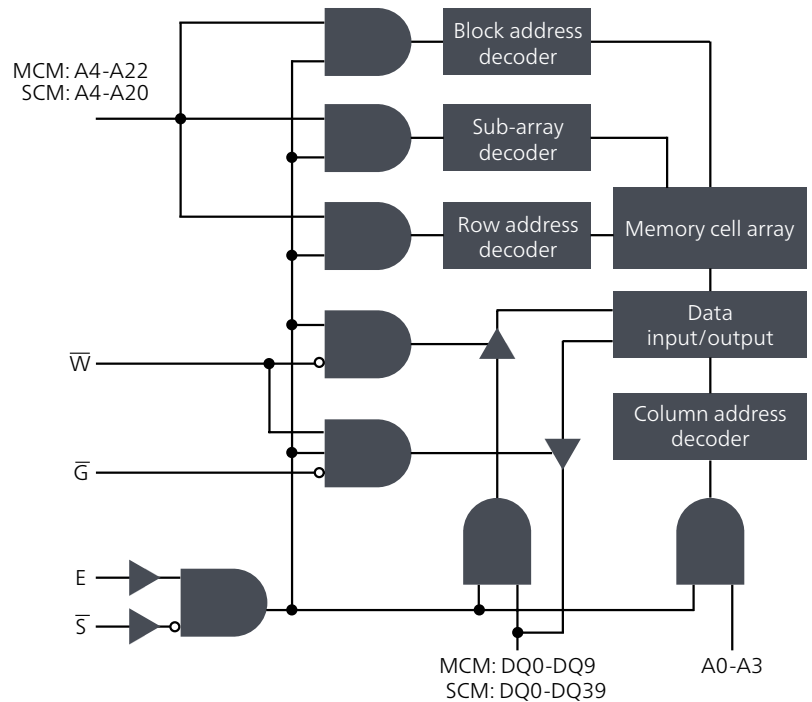
**DQ:** 0-9 (MCM) or 0-39 (SCM) bi-directional data pins that serve as data outputs during a read operation and as data inputs during a write operation.

**S** negative chip select at a low level allows normal read or write operation. At a high level, S forces the SRAM to a pre-charge condition, holds the data output drivers in a high-impedance state, and disables only the data input buffers. If this signal is not used, it must be connected to GND.

**W** negative write enable at a low level activates a write operation and holds the data output drivers in a high-impedance state. At a high-level, W allows normal read operation.

**G** negative output enable at a high level holds the data output drivers in a high-impedance state. At a low level, the data output driver state is defined by S, W, and E. If this signal is not used, it must be connected to GND.

**E** chip enable at a high level allows normal operation. At a low level, E forces the SRAM to a pre-charge condition, holds the data output drivers in a high-impedance state, and disables all the input buffers except the S input buffer. If this signal is not used, it must be connected to VDD.



## Specifications

Monolithic 80 Mb family of products

80 Mb single-chip (monolithic), up to 320 Mb multi-chip modules (MCM) available  
 – 2M x 40 (monolithic)  
 – 8M x 40 (MCM)

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