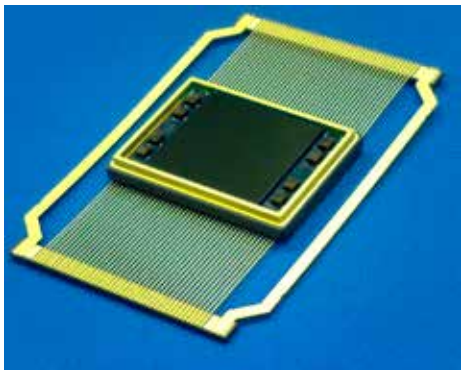
BAE SYSTEMS

Monolithic 64M radiation-hardened SRAM



High-speed memory product

The monolithic 64 Mb static random access memory is BAE Systems' next generation, high-density memory product for users in the space community.

Description

Capable of withstanding the effects of natural space and an upper radiationhardened environment, the 64 Mb monolithic SRAM has a total-dose tolerance of greater than 100Krad and an upset rate of less than 1E-11 upsets per bit-day.

Key features

- Read/write access time 12.5 ns typical, 17 ns and 20 ns worst case
- Operating temperature range -55 degrees celsius to 125 degrees celsius
- Operating voltage (core) 1.2 V
- Operating voltage (I/O) 1.8 V, 2.5 V
- Standby power < 7 mW typical, < 265 mW worst case
- Operating power < 4 mW/MHz typical
- Packaging 86-lead ceramic flatpack
- Asynchronous operation
- Prototype and flight flows
- Latchup-immune

System definitions

A:0-22 Address input pins that select a particular 8-bit word within the memory array.

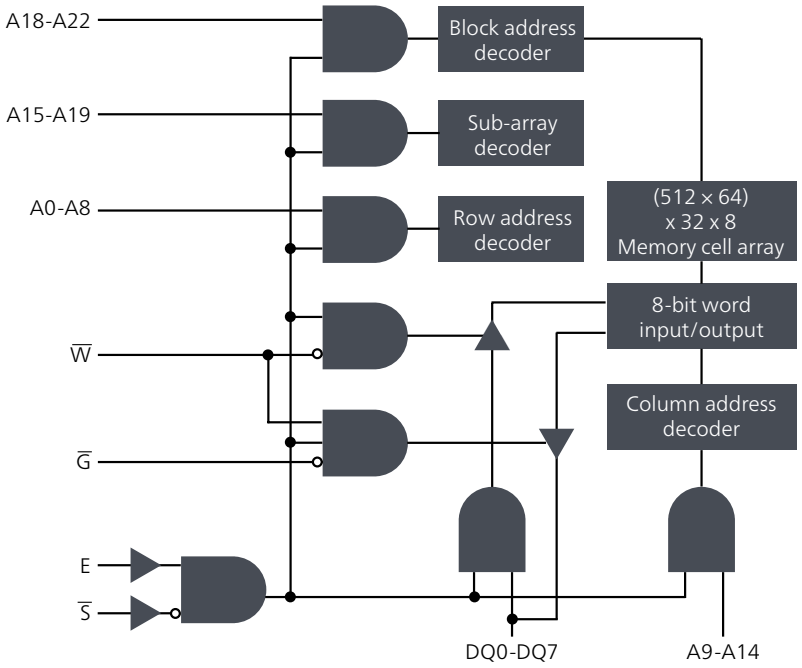
DQ:0-7 Bi-directional data pins that serve as data outputs during a read operation and as data inputs during a write operation.

S Negative chip select at a low level allows normal read or write operation. At a high level, S forces the SRAM to a precharge condition, holds the data output drivers in a high-impedance state, and disables only the data input buffers. If this signal is not used, it must be connected to GND.

W Negative write enable at a low level activates a write operation and holds the data output drivers in a highimpedance state. At a high-level W allows normal read operation.

G Negative output enable at a high level holds the data output drivers in a highimpedance state. At a low level, the data output driver state is defined by S, W, and E. If this signal is not used, it must be connected to GND.

E Chip enable at a high level allows normal operation. At a low level, E forces the SRAM to a precharge condition, holds the data output drivers in a high-impedance state, and disables all the input buffers except the S input buffer. If this signal is not used, it must be connected to VDD.



Specifications

Monolithic 64 Mb family of products	64 Mb single-chip, up to 320 Mb multi-chip modules available – 2M x 32 (monolithic) – 8M x 40 (MCM) 64 Mb SRAM single-chip die are organized in either 8M x 8 or 2M x 32 formats, packaged in an 86-lead ceramic flatpack.

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