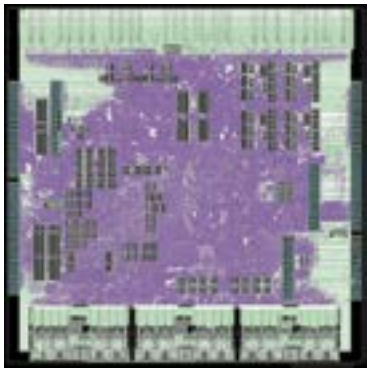
BAE SYSTEMS

RADNET™ family of radiation-hardened products

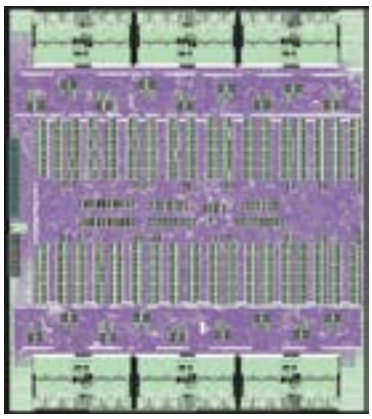
The **RADNET™** family of radiation-hardened application specific standard products (ASSP) includes a wide spectrum of network fabric components that provide mix-and-match capabilities for high-performance interconnections between space electronic elements.

Description



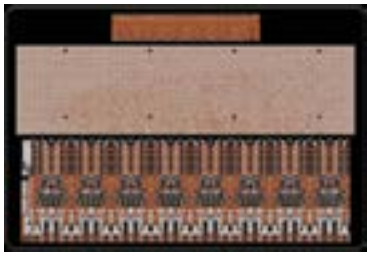
RADNET SRIO-EP ASSP die layout

The **RADNET™ SRIO-EP ASSP** provides connections between the RapidIO Revision 2.1 fabric and alternate interfaces along with access to various memory capabilities external to the ASSP. Alternate interfaces include two XUAI high-performance serial link interfaces and lower bandwidth legacy protocol interfaces (four SpaceWire ports, four Inter-integrated circuit (I2C) ports, a serial peripheral interface (SPI), a 32-bit peripheral component interconnect (PCI) Bus, discretes, a MIL-STD-1553B dual-redundant controller, two JTAG master ports, a 32-bit SelectMAP interface, and test and debug interfaces). The SRIO-EP also offers access to two DDR3 SDRAM controllers, a flash memory controller, an EEPROM interface, an internal 4 KB priority scoreboard and 256 KB of internal SRAM.



RADNET 1848-PS ASSP die layout

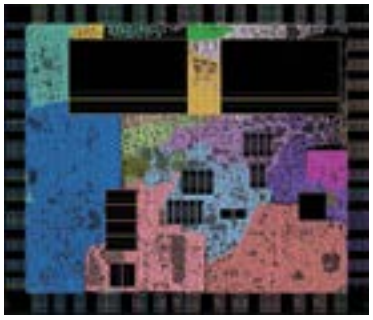
The **RADNET™ 1848-PS ASSP** enables high-performance serial RapidIO revision 2.1 packet switching to up to 18 ports across 48 lanes, enabling larger on-board RapidIO networks. Based on the Integrated Device Technology (IDT) CPS-1848™ switch product, the 1848-PS uses user-programmable ports of flexible width, allowing support for up to 12 four-lane ports or 18 ports of varied widths (combinations of 1x, 2x and 4x) across a non-blocking crossbar. Switch capabilities include short and long-run support, pseudo-random binary sequence generation, programmable post- and pre-emphasis, transmitter and receiver-based flow control, multicast support, and individual port control and reset. I2C primary/replica interfaces are provided, along with joint test action group test and debug capabilities, which may configure any interface either autonomously or under external control.



RADNET 1616-XP ASSP die layout

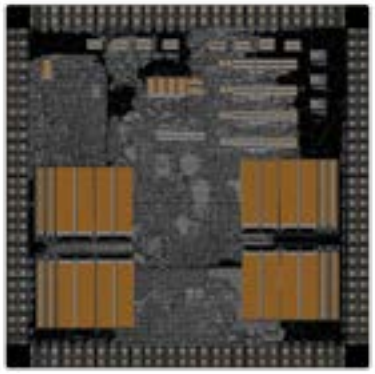
The **RADNET™ 1616-XP ASSP** provides protocol-agnostic connections to support use with serializer / deserializer based protocols such as Aurora, XAUI and RapidIO®. The 1616-XP provides broadcast, multicast, and unicast circuit switching for 16 input to 16 output SerDes lanes on a lane-by-lane basis with low latency and lower power than packet switches. Receivers have programmable input equalizers and automatic termination calibration. Drivers have programmable de-emphasis and output drive levels with integrated 50 Ohm output impedance. I2C and JTAG interfaces are provided for configuration, test, and debug.

Description



RADNET SpW-EP ASSP die layout

The **RADNET™ SpW-EP ASSP** enables a low-power, high-performance connection between SpaceWire fabric, remote instruments, and peripherals through a variety of matched interfaces. Interfaces include a dual-redundant 256 Mb/s SpaceWire port, a 32-bit bidirectional first-in, first-out interface, discretes, a 16-bit SelectMAP interface, two I2C ports, one service provider interface, one universal-asynchronous receiver-transmitter and JTAG primary, and replica interfaces for test and debug. A 32-bit embedded RISC microprocessor assists with data movement and protocol execution. The SpW-EP provides memory access to a 32-bit SRAM/PROM interface and 32 KB of internal SRAM. Power dissipation is typically between 0.1 to 1.4 Watts, depending on speed and interfaces in use.

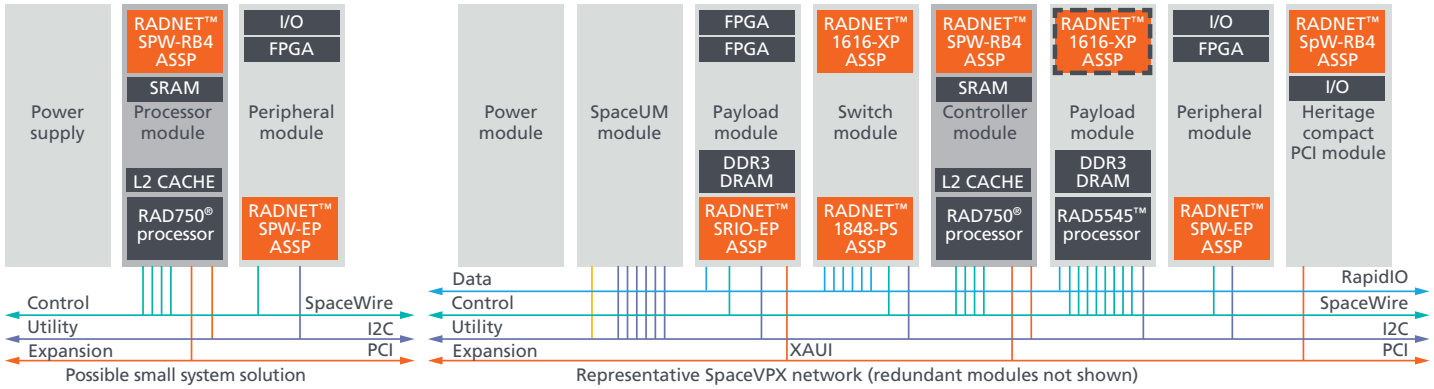


RADNET SpW-RB4 ASSP die layout

The **RADNET™ SpW-RB4 ASSP** provides connections between four ports of SpaceWire fabric and alternative interfaces with access to large memory capacity. This general purpose connection device may also serve as a processor bridge to processors in the RAD750® family. Interfaces include four 256 Mb/s SpaceWire ports, a 64-bit 66 MHz PCI Bus, a 32-bit 33 MHz PCI Bus, discretes, a dual redundant MIL-STD-1553B controller, a 32-bit FIFO interface, one UART, and a dual JTAG interfaces for test and debug. The SpW-RB4 also provides direct access to 96 KB of internal SRAM and up to 4 GB of external SRAM/PROM/SDRAM with selectable parity, nibble, or Reed Solomon error correcting code. A 32-bit embedded RISC microprocessor assists with data movement and protocol execution.

Together, these five RADNET ASSPs form the basis for current and future high-performance SpaceVPX modules that leverage its fabrics to move data efficiently between space electronic assemblies. All RADNET™ family products are designed to operate seamlessly with our RAD750® processor and RAD5545™ system-on-chip as well as future processor products.

Hardware block diagram



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