

Eclipse RF™ Products

RXR6644



The **RXR6644**, is a quad-channel wideband tuner and digital receiver operating in the HF, VHF, and UHF bands between 100 kHz and 6 GHz. Its analog tuners and digital receiver motherboard are integrated in a rugged, conduction-cooled 6U VPX module. Leveraging the RF and digital assemblies common to the entire line of R6000 receivers, the RXR6644 reduces manufacturing costs and improves production. It is designed for use in embedded applications where size, weight, and power (SWaP) are important factors.

The RXR6644 is a member of the R6000 line of receivers from BAE Systems' Eclipse RF™ products. BAE Systems has been developing and manufacturing high-performance tuners, digital receivers, time/frequency reference modules, antenna distribution modules and complete hardware suites for the SIGINT market for more than 25 years.

Key features and benefits

- Four wideband RF inputs per 6U 1 inch VPX slot improves channel density
- Increased tune range of each RF channel provides wider spectral coverage per VPX slot
- Maximum instantaneous IF bandwidth enables wider spectral coverage per RF channel
- 6U VPX form-factor offers more board space than 3U modules, supporting higher density FPGAs for back-end filtering and digital signal processing applications
- Up to three Xilinx Kintex Ultrascale 60 FPGAs may be populated on the receiver motherboard providing the system integrator a trade-off between module cost and considerable user-defined processing resources
- Sub-octave pre-selectors decrease intermodulation products, improving dynamic range and overall system performance
- Adherence to open standards such as VITA-65 OpenVPX, VITA-48 VPX REDI and VITA-67 blind-mate RF ensure interoperability with other sub-system components, reducing integration and life-cycle management costs

RXR6644 specifications

Radio frequency (RF)

| | |
|-------------------------------|---|
| Tuning frequency range | 100 kHz to 6 GHz |
| RF tuning resolution | 1 MHz via first LO |
| RF tune speed | Consult factory |
| Analog IF bandwidth | Selectable 80/10 MHz (80/40, 60/10, 60/40 MHz optionally available) |
| Input impedance | 50 ohms |
| VSWR | Less than 2.5:1 |
| Preselection 100kHz to 90 MHz | Bypass, 100 kHz-20 MHz, 20-30 MHz and 30-90MHz |
| 90MHz to 6 GHz | Suboctave preselectors |
| Max input level | + 24 dBm |
| Image rejection | > 80 dB |
| IF rejection | > 80 dB |
| LO re-radiation | < -90 dBm |
| Noise figure | 14 dB typical (8 dB with pre-amp selected) |
| Third order intercept | + 3 dBm minimum, + 5 dBm typical |
| In-band of final IF (IIP3) | +24 dBm minimum, +30 dBm |
| Out of band | Typical at 0 dB attenuation, two tone |
| Second order intercept | +45 dBm minimum, +50 dBm typical |
| Single tone SFDR | > 83 dB with tone at -1 dBFS |
| Internal spurious | < -110 dBm typical |
| Coherency | Daisy chain distribution of first and second LOs for N channel |

External reference

(Recommended minimum performance specifications)

| | |
|-----------------------|------------------------------|
| Frequency | 10 MHz +/- 5 PPM or better |
| Amplitude | 0 dBm +/- 3 dBm |
| Harmonics | -20 dBc maximum |
| Non-harmonic spurious | -80 dBc maximum |
| Source VSWR | 1.5:1 (reference to 50 ohms) |

Digital specifications

| | |
|---------------------|--|
| Wideband data | 16-bit real or 32-bit complex at selected sample rate |
| Filtered narrowband | 16-bit IQ serial at sample rate determined by selected bandwidth |
| Output sample rate | Set by selected re-sampler (10, 80, 40 and 12.8 cMSPS) |
| Narrowband DDCs | 32 narrowband DDCs each accessible by either RF channel (bandwidths >1.2 MHz may reduce this number) |
| Gain control | AGC and MGC modes |
| steps | Attenuation range 45 dB with 1 dB Fast attack Slow decay Freeze Dump-attack freeze Manual setting (MGC) |
| Demodulation | AM, FM, USB, LSB, CW OOK, uLaw or aLaw TDM output |
| Delay memory | 250 MB per input channel |
| Sync I/O | Daisy chained distribution optional |
| Timing coherency | A/D sample coherency provided by LO daisy chaining |

Mechanical/environmental specifications

| | |
|-----------------------|--|
| Size | 6U-160 VPX 1 inch pitch |
| Weight | 3.6 pounds |
| Power | 150 Watts minimum, 200 Watts maximum Power dissipation most highly determined by FPGA utilization |
| Cooling | Conduction cooled to siderails or air cooled |
| Operating temperature | System integrator must ensure rail temperatures remain between -20 and +70 degrees Celsius |

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