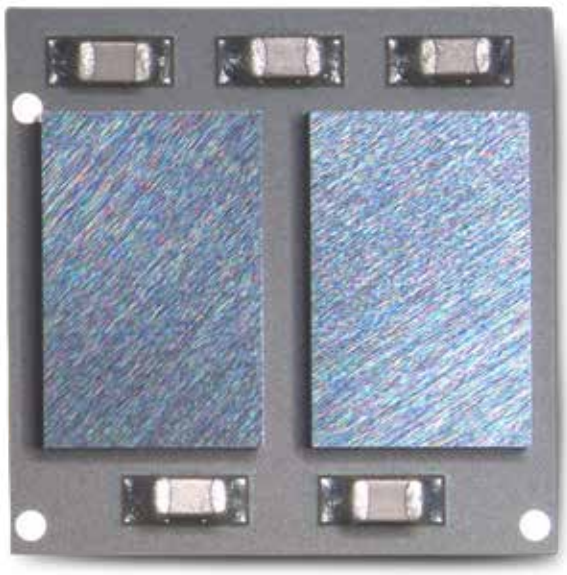
BAE SYSTEMS

128 Mb radiation-hardened SDRAM

High-speed memory product

The monolithic static random-access memory (SRAM) bit cell array coupled with a double data rate third generation low voltage (DDR3L) synchronous dynamic random-access memory (SDRAM) interface is BAE Systems' next generation RHBD (Rad Hard by Design), ultra-high-speed memory product for users in the space community.

Capable of withstanding the effects of natural space and an upper radiation hardened environment, the monolithic 128 Gb SDRAM has a total-dose tolerance of greater than 300 Krad and an upset rate of less than 1E-07 upsets per bit-day.



Pre-production 128 Mb SRAM prior to final assembly

Key features

- Operating temperature range -55 °C to 125 °C
- Operating voltage (core) of 0.80 ±0.5V
- Operating voltage (I/O) of 1.8 ±0.5V
- Access time 5.4 ns; 133.33 MHz
- Radiation-Hardened By Design (RHBD) 12nm Bulk FinFET CMOS
- Packaging 81 BGA multi chip module
- Synchronous operation
- Prototype and flight flows
- Latchup immune

System definitions

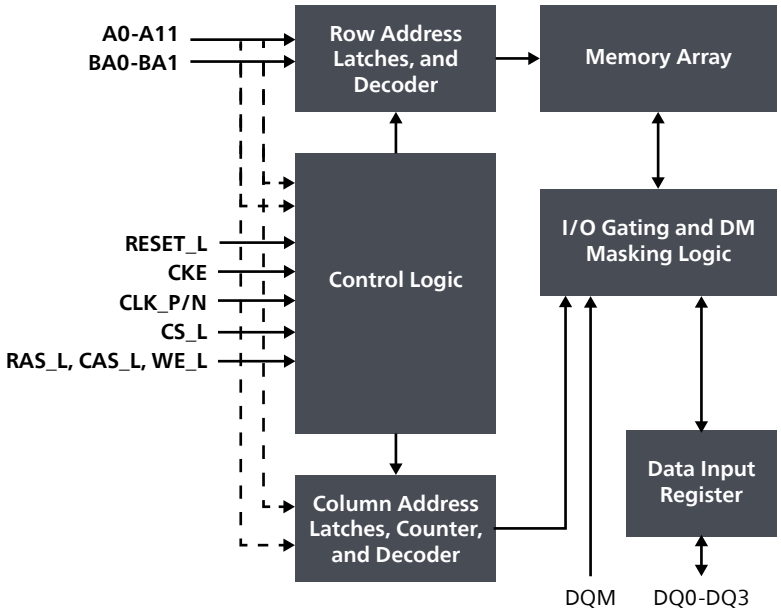
BA: 0-1 BA(1:0) define the bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA(2:0) define which mode register is loaded during the MODE REGISTER SET command.

A: 0-11 Address pins provide the row address for ACTIVATE commands, and the column address and auto precharge bit (10) for READ/WRITE commands, to select one location out of the memory array in a respective bank.

CS_L: Enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS_L is registered HIGH.

RAS_L, CAS_L, WE_L: Command inputs to the command decoder used to specify the various commands.

DQ: 0-7 Bi-directional data pins that serve as data outputs during a READ command and as data inputs during a WRITE command. DQ(0:3) and DQ(4:7) for die 0 and die 1.



DQS_P, DQS_N: Bi-directional data strobe that are edge-aligned output with read data and center aligned input with write data.

CKE: Enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the SDRAM.

RESET_L is an active low CMOS input. RESET_L assertion and desertion are asynchronous.

DQM: An input mask signal for write data. Input data is masked when DM is sampled HIGH along with the input data during a write access.

CLK_P, CLK_N: Differential clock inputs that sample all control and address input signals upon the crossing of the positive edge of CLK_P and the negative edge of CLK_N.

Specifications

128 Mb DDR3L SDRAM operation family of products	64 Mb single chip (die), up to 128 Mb multi-chip module (MCM) is available in – 16M x 4 (die) – 16M x 8 (MCM)

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