

# Radiation-hardened DDR3L SRAM products

## Ultra-high-speed memory products

The monolithic static random-access memory (SRAM) bit cell array coupled with a double data rate third generation low voltage (DDR3L) synchronous dynamic random-access memory (SDRAM) interface is BAE Systems' next generation RHBD (Rad Hard by Design), ultra-high-speed memory product for users in the space community.

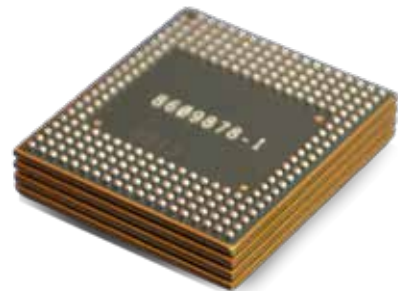
Capable of withstanding the effects of natural space and an upper radiation hardened environment, the monolithic SRAM DDR3L SDRAM has a total-dose tolerance of greater than 300Krad and an upset rate of less than  $1E-12$  upsets per bit-day.



Pre-production 1Gb SRAM in side-by-side two die format

## Key features

- Transfer rate of 800 MT/s
- Operating temperature range -55 °C to 110 °C
- Operating voltage (core) of  $0.80 \pm 0.5V$
- Operating voltage (I/O) of  $1.35 \pm 0.5V$
- RHBD 12nm Bulk FinFET CMOS
- On Die Error Detection and Correction (EDAC)
- 1GB Packaging 201-pin Hermetic Ceramic Column Grid Array (CCGA) and 2GB Packaging 237-pin Plastic Ball Grid Array (PBGA)
- Synchronous operation
- Prototype and flight flows
- Immune to Latchup and SEFI
- Only RHBD DDR3 Memory on the market



Pre-production 2Gb SRAM in stacked, four die format

## System definitions

**BA:** 0-2 BA(2:0) define the bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA(2:0) define which mode register is loaded during the MODE REGISTER SET command.

**A:** 0-12 Address pins provide the row address for ACTIVATE commands, and the column address and auto precharge bit (10) for READ/WRITE commands, to select one location out of the memory array in a respective bank.

**CS\_L:** 0-1 Enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS\_L is registered HIGH. One per die (die 0 and die 1).

**RAS\_L, CAS\_L, WE\_L:** Command inputs to the command decoder used to specify the various commands.

**DQ:** 0-7 Bi-directional data pins that serve as data outputs during a READ command and as data inputs during a WRITE command.

**DQS\_P, DQS\_N:** Bi-directional data strobe that are edge-aligned output with read data and center aligned input with write data.

**CKE:** 0-1 Enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the SDRAM.

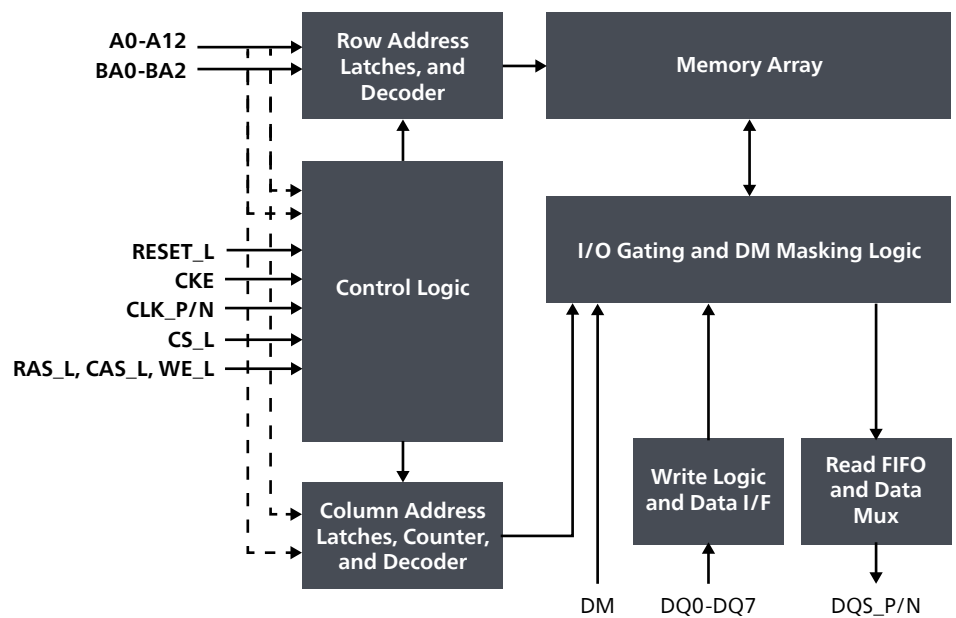
**RESET\_L** is an active low CMOS input. RESET\_L assertion and desertion are asynchronous.

**SEL\_PRECH\_ENA:** When high, the selective precharge function is enabled—internal RAM RET1N pins are set to '1' when selected by an ACTIVE command and set to '0' by a PRECHARGE or AUTO PRECHARGE command.

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**DM:** An input mask signal for write data. Input data is masked when DM is sampled HIGH along with the input data during a write access.

**CLK\_P, CLK\_N:** Differential clock inputs that sample all control and address input signals upon the crossing of the positive edge of CLK\_P and the negative edge of CLK\_N.



## Specifications

1GB and 2Gb SRAM DDR3L SDRAM operation family of products

512 Gb single chip (die), up to 2 Gb multi-chip module (MCM) is available in  
 – 128M x 8 (MCM) (1 Gb)  
 – 64M x 32 (MCM) (2 Gb)

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