The MATRICs RF-FPGA in 180nm SiGe-on-SOI BiCMOS

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***Abstract*—MATRICs (Microwave Array Technology for Reconfigurable Integrated Circuits) is a DC-to-20 GHz general purpose reconfigurable array of RF circuits embedded in a flexible switch fabric. Fabricated in a commercial SiGe-on-SOI BiCMOS process, the MATRICs IC employs SiGe HBTs for high-linearity (> + 10 dBm IIP3) amplification and low phase-noise frequency generation, and SOI FETs for low-loss switching. It achieves high on-chip RF isolation (>80 dB at 16 GHz) due to the high-resistivity SOI substrate, differential signalling, and chip-scale flip-chip bump packaging. MATRICs will allow fixed-function RF systems to have the size, weight, and power benefits of a custom RF ASIC without the associated long development cycle and high NRE, and enable future RF subsystems to be dynamically reconfigured on-the-fly, adapting to changing environments.**

***Index Terms*— RF-FPGA, reconfigurable, switch matrix, N-path filter, SiGe-on-SOI BiCMOS, PLL.**

I. Introduction

Much of the commercial RFIC industry is driven by high-volume applications such as mobile phones and portable computing, where low per-unit cost and low dc power consumption are achieved by developing full-custom system-on-chips (SoCs) in advanced CMOS process nodes. These SoC development efforts require large engineering teams, and have multi-million dollar fabrication costs due primarily to the fine-geometry CMOS mask expense.

In contrast, many military systems require ASIC size and weight, but do not require a large number of units and therefore cannot amortize the expense of custom ICs in fine-geometry CMOS. Still, raw performance is critical, as military systems must operate in hostile RF environments, so linearity, spectral purity, and interference rejection are of utmost importance. The MATRICs RF-FPGA IC described in this paper, fabricated in a commercial 180nm SiGe-on-SOI process [1], seeks to address these demanding requirements across a wide range of applications while minimizing non-recurring engineering (NRE) expense.

II. MATRICs RF-FPGA Architecture

Analogous to a digital FPGA, the MATRICs RF-FPGA contains an array of reconfigurable RF blocks embedded in a flexible switch fabric (Fig. 1). Amplification, filtering, frequency conversion, and frequency generation are all included on the MATRICs IC, along with on-chip digital control and state memory. Unused blocks can be powered off and bypassed. Individual blocks have many (50 to 100) bits of fine-grained control, allowing gain, BW, linearity, center frequency, etc. to be adjusted statically,

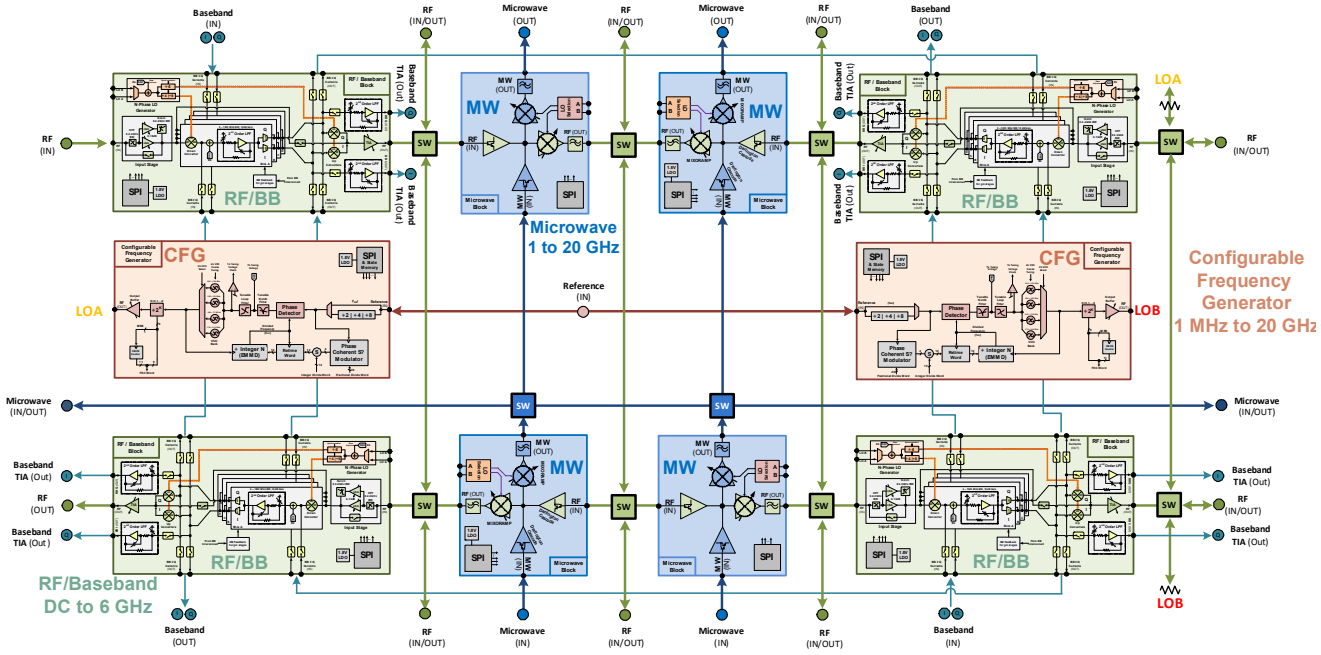
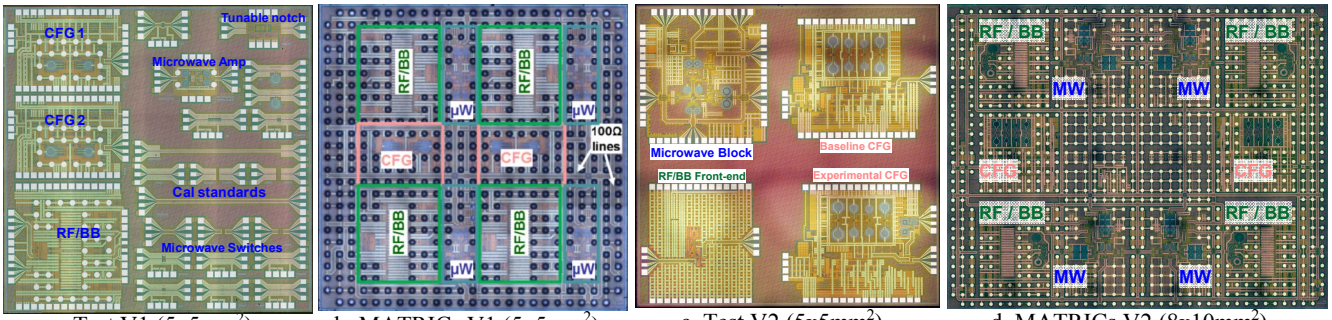


Fig. 1. MATRIC V2 Architecture



a. Test V1 (5x5mm^2) b. MATRICs V1 (5x5mm^2) c. Test V2 (5x5mm^2) d. MATRICs V2 (8x10mm^2)

Fig. 2. First- and second-generation MATRICs RF-FPGA ICs.

after power-up, or dynamically, for on-the-fly reconfiguration. Similarly, the switch fabric interconnecting the blocks is also controlled by local, per-block, SPI and state memory.

Two generations of MATRICs RF-FPGAs have been developed along with additional test chips containing individual block break-outs (Fig.). The full-up MATRICs ICs contain four 1-to-20 GHz Microwave blocks (MW), four DC-to-6 GHz RF/Baseband blocks (RF/BB), and two

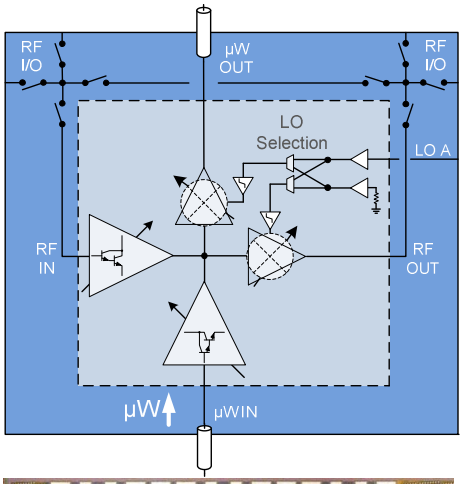


Fig. 3. Microwave block (Test V2 IC)

0.01-to-20 GHz Configurable Frequency Generator (CFG) blocks. Most RF and baseband signals are differentially routed on chip, with the higher-frequency signals distributed by differential 100Ω grounded CPW transmission lines. Local Oscillator (LO) signals generated by the CFGs employ open-collector CML gates with load-side-only terminations (to save DC power while maximizing signal swing). Wherever signals cross, shielded RF cross-unders are employed to maintain isolation, with greater than 80 dB of isolation demonstrated at 16 GHz (in the MATRICs V1 chip). While the test chips are designed for wafer-probe, the MATRICs die are bumped and flip-chip mounted, providing low-impedance power supplies, low-parasitic RF connections, and superior RF isolation.

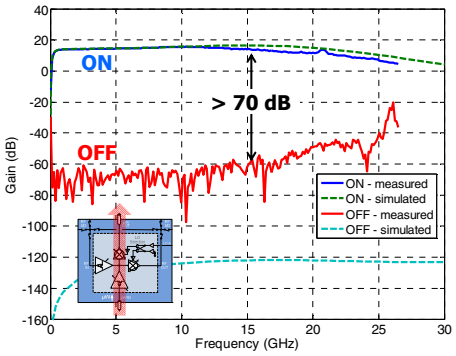
III. Block Design and Performance

Design and performance of the Microwave and RF/Baseband blocks are included in this section. The Configurable Frequency Generator has been submitted separately for publication [2] and is not discussed here.

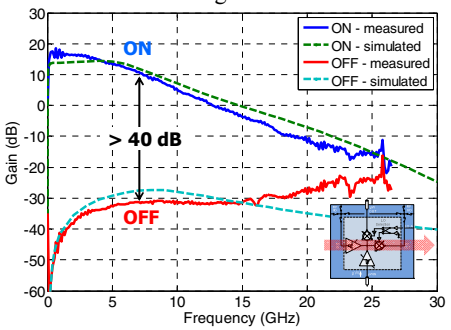
A. Microwave Block (MW)

The MATRICs V2 chip (and Test V2 chip) includes a multi-function 1-to-20 GHz Microwave block (Fig. 3). In addition to amplification and frequency conversion, the Microwave block acts as an active 4-way switch, routing signals between adjacent blocks. The MW block has two inputs and two outputs: DC-to-6 GHz input and output, designed to interface with adjacent RF/Baseband blocks, and 1-to-20 GHz microwave input and output, designed to interface with other MW blocks or off-chip signals. The input stages of the MW block employ a Darlington feedback configuration for wideband, linear operation. The outputs of these input stages converge at a common-node in the center of the MW block, before exiting the MW block through one of two MIXORAMP output stages. As the name implies, the MIXORAMP stages can be configure as amplifiers or up/down conversion mixers.

At any given time, only one input stage and one output stage are powered up, with the off stages acting as active isolators. The "vertical" microwave path has a minimum



a. MW-to-MW gain and isolation



b. RF-to-RF gain and isolation

Fig. 4. Microwave block as amplifier or switch.
MW: 1 to 20 GHz; RF: DC to 6 GHz

of 70 dB on/off ratio to 15 GHz (Fig. 4a), while the "horizontal" RF path has better than 40 dB of on/off ratio out to 6 GHz (Fig. 4b). These ON/OFF ratios compare quite favorably to most passive switch designs.

Signals may also enter the (left) RF input and exit through the (top) MW output, or enter the (bottom) MW input and exit the (right) RF output. Noise figure remains under 9 dB in any of these amplifier configurations. As a mixer, the MW block conversion gain is between 8 to 15 dB (depending upon the frequencies at the 3 ports), with a noise figure between 12 and 13 dB.

B. RF/Baseband Block (RF/BB)

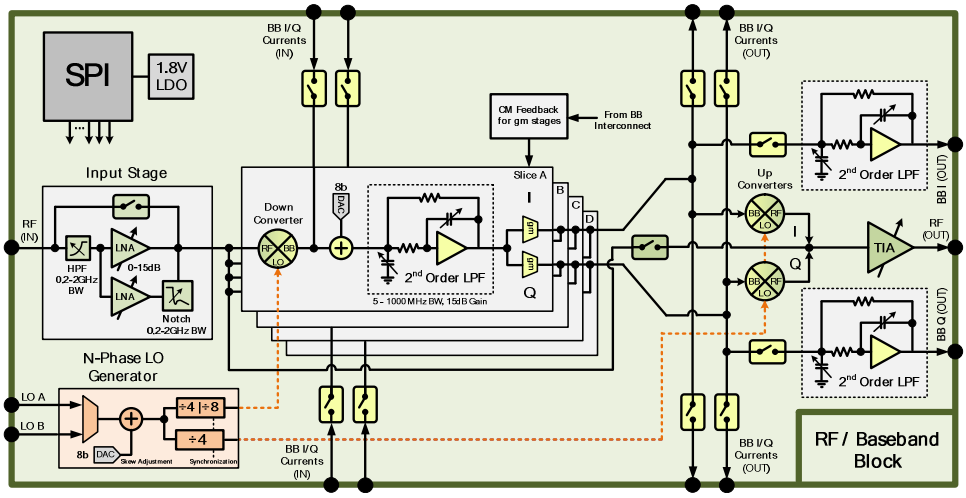
The DC-to-6GHz RF/Baseband block (Fig. 5) performs RF amplification and filtering, down-conversion, baseband gain and filtering, upconversion, and signal routing. The input stage of the RF/BB is reconfigurable, with switchable gain and RF filtering, and can be bypassed for high-linearity mixer-first operation.

The middle stage of the RF/BB block can be configured for 4-path I/Q or 8-path harmonic-reject downconversion, or bypassed entirely. Its SiGe HBT CML-based N-phase LO generator allows the RF/BB block to achieve outstanding 3rd- and 5th-harmonic rejection in 8-path mode (Fig. 6), at the expense of DC power. For narrow-band applications, or operation above 3 GHz, 4-path mode can be used, reducing the DC power significantly.

The RF/BB block performs filtering both at RF and baseband. As a direct-downconversion receiver, the RF/BB block's N-path filtering tracks the LO frequency and can therefore be tuned precisely by tuning the LO.

The output stage of the RF/BB block provides further gain and filtering, and can also be configured to perform I/Q upconversion. Multiple RF/BB blocks may be cascaded either at RF or at baseband to achieve additional gain and filtering.

Table I compares the RF/Baseband block (in downconversion mode) to recent research results of similar N-path or harmonic-reject receivers. The MATRICs chips reported here operate over a much wider range of instantaneous bandwidths and achieve superior in-band (IB) and out-of-band (OOB) linearity. This level of performance was achieved primarily by employing SiGe HBTs, which results in significantly higher power consumption compared with the other research results.



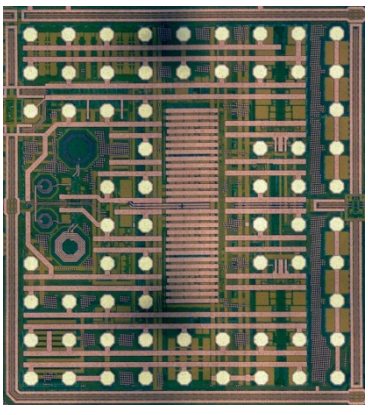


Fig. 5. DC-to-6 GHz RF/Baseband Block (MATRICs V2)

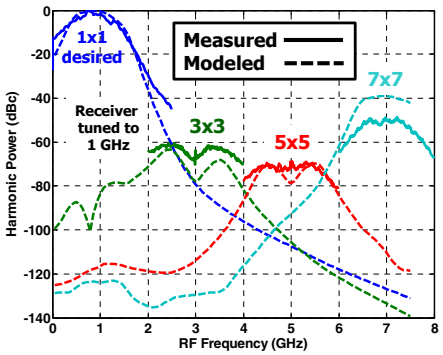


Fig. 6. RF/Baseband block harmonic rejection in 8-path mode, with on-chip pre-filter set to ~ 2 GHz. Measured in Test V1 IC.

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TABLE I

COMPARISON OF RF/BASEBAND BLOCK IN N-PATH DOWNCONVERSION MODE TO RECENT RESEARCH.

	[3]	[4]	[5]	[6]	[7]	[8]	This work MATRICs V1[1]	This work MATRICs V2[2]
Technology	65nm CMOS	65nm CMOS	40nm CMOS	40nm CMOS	65nm CMOS	40nm CMOS	SiGe-on-180nm SOI CMOS	
Frequency (MHz)	100 - 2400	850, 900, 1800, 1900	80 - 2700	400 - 6000	500 - 3000	1800 - 2400	20 - 6000	
Instantaneous BW (MHz)	1	4	2	1.5 to 20	8 to 57 (?)	1	20 - 1500	10 - 2000
3rd/5th Harmonic Reject. (dB)	35-43 (<500MHz)	44/?	42/45	none	46/51	54 / 65	60/70 (8-path, with on-chip tunable pre-filter, <3 GHz)	
Image Rejection (dB) (un-calibrated)	-	-	-	-	-	-	> 48 dB over 20 MHz BW > 40 dB over 1 GHz BW	
Max Gain (dB)	70	60	72	70	35	45	45 dB per RF/BB	
NF (dB)	7	2.9	2 - 12	3-9, LNA 1st 7-15, mix 1st	5.5 – 8.8	2 – 3.5	10 - 12.5, LNA 1st 15 to 21, mix 1st	
IB IIP3 (dBm)	< -40	0	< -20	+6	-12	-	-5 , LNA-1st +5, mix-1st	+6, LNA-1st +16, mix-1st
OOB IIP3 (dBm)	+25	-	+13.5	+10	+11	+18	+12 , LNA-1st +28, mix-1st	+20, LNA-1st +35, mix-1st
OOB IIP2 (dBm)	+56	+50	+54	+30 un-cal'd +70 cal'd	+46, un-cal'd	+64	+40 un-calibrated	
$P_{blocker\_OOB}$ for CP_{-1dB} (dBm)	-	+1	-2	-8	-1	0	-10 to + 7	TBD
Power Consumption (mW)	37-70	240	35-78	55	250 - 600	32	1000 to 1500	800 to 2000
Supply Voltages	1.2, 2.5	2.5	1.3	1.1, 2.5	1.2, 2.5	1.2, 1.8	1.8, 3.3	
Active Area (mm^2)	2	1.4	1.2	2	5.9	0.74	2.2	4.1

[1]Measured [2]Simulated