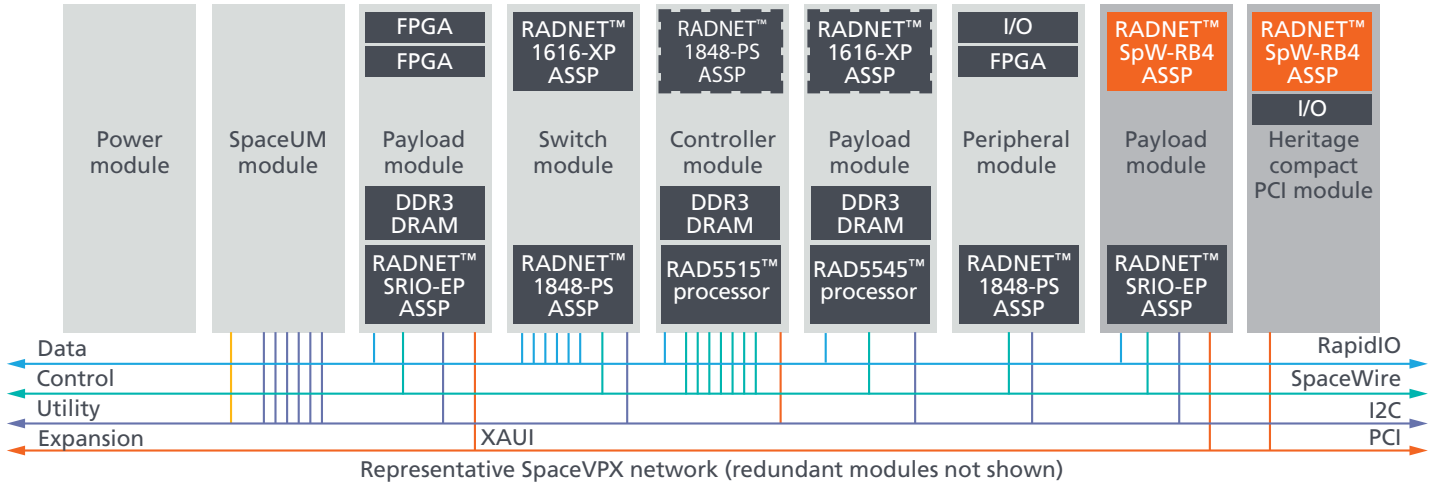
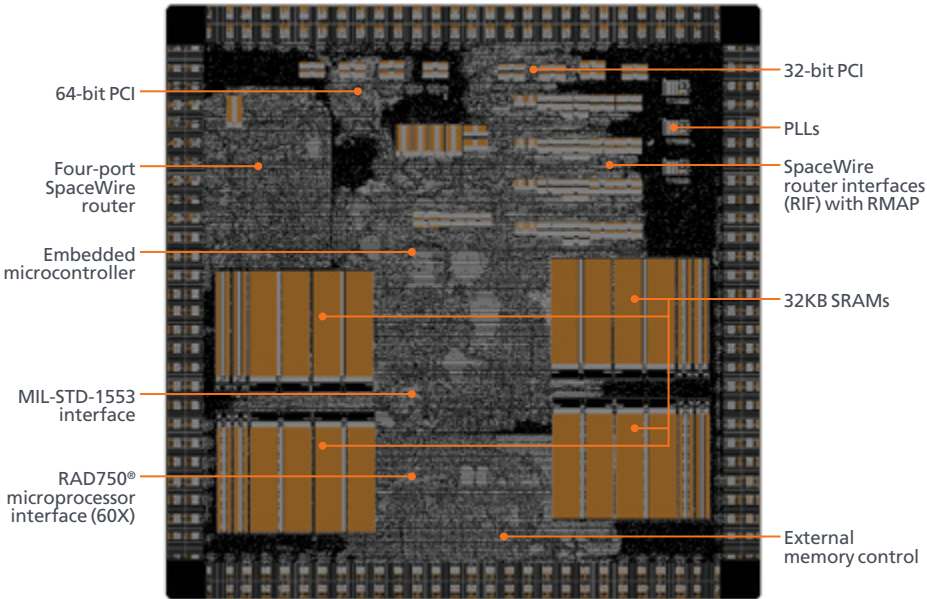


RADNET™ SpW-RB4 radiation-hardened SpaceWire four-port router microcontroller-based bridge

The RADNET SpW-RB4 application specific standard product (ASSP) provides connection between SpaceWire fabric and alternative interfaces along with access to large capacity SRAM/DRAM memory.

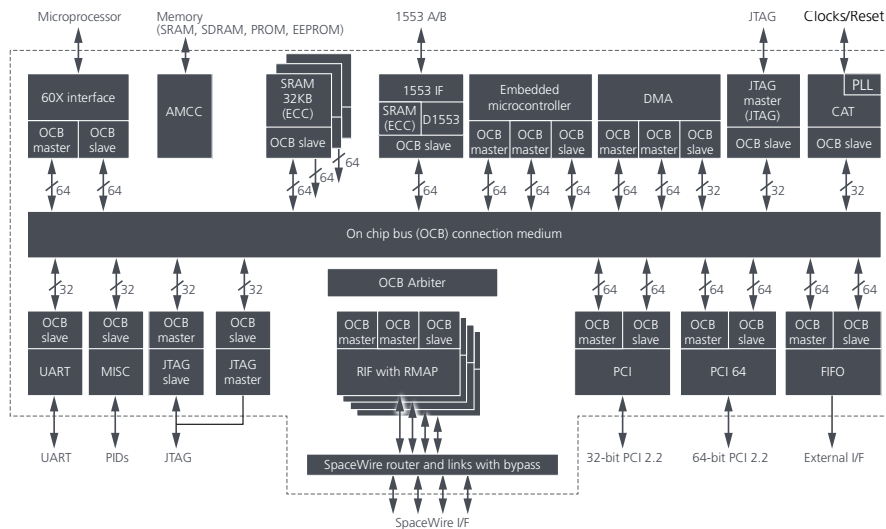
The RADNET SpW-RB4 ASSP is a member of the RADNET family of high-performance radiation-hardened networking products. An extremely flexible, general purpose connection device and processor bridge ASSP, it integrates a wide variety of interfaces and is compatible with the SpaceVPX standard.



Key features and benefits

- Embedded controller provides support for protocol extensions and I/O management
- Remote Memory Access Protocol (RMAP) support for using SpaceWire as a medium speed data plane or expandable control plane
- UART, JTAG, and bi-directional FIFO interface connections
- Configurable error detection and correction codes include parity, single bit error correction/double bit error detection (SEC/DED), nibble detect and correction, and Reed Solomon coding across up to 32 additional bits
- 96 KB of SRAM with SEC/DED error correction
- Up to 18 Dhrystone MIPS (DMIPS) to support protocol extensions, command and data handling, processor monitoring, and configuring capabilities
- 60X interface for bridging to I/O and memory from the RAD750 microprocessor family
- Dual peripheral component interconnect (PCI) interfaces (32/64- bits wide) are provided for onboard and backplane connections to legacy devices
- MIL-STD-1553B interface provides off card legacy connections

Hardware block diagram



For more information contact:

BAE Systems
 9300 Wellington Road
 Manassas, Virginia 20110-4122
T: 571 364 7777
E: space.contact@baesystems.com
W: baesystems.com

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Specifications

Technology	Radiation-hardened by design RH15™ circuit library Trusted foundry 150 nm CMOS process 1144-pin, 35 mm ceramic column grid array package
Temperature	Operating at -55 to +125 degrees Celsius
Radiation-hardness	Total ionizing dose: 1 Mrad (Si) Single event upset (SEU): <1E-10 upsets/bit-day Latch-up immune
Power supply	1.5 V +/- 5 percent core 3.3 V PCI, low voltage differential signaling (LVDS) and CMOS I/O
Power dissipation	2-6 watts at 95 degrees Celsius and +5 percent voltage; depends on combination of active interfaces Unused interfaces can be disabled
Interfaces	
Memory	4GB SRAM/PROM/SDRAM interface with selectable parity, nibble or Reed Solomon error correcting code
Input/output	Four external SpaceWire ports with integrated router; up to 320 Mbaud/lane Four internal SpaceWire ports support DMA-controlled RMAP access to the internal registers and memory 60x processor interface 64-bit, 66 MHz parallel PCI bus 32-bit, 33 MHz parallel PCI bus 36 discretes with clocks and timers MIL-STD-1553B with A/B transceiver Bi-directional FIFO interface 16550 UART interface
	Test and debug Dual JTAG master interface

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