BAE SYSTEMS

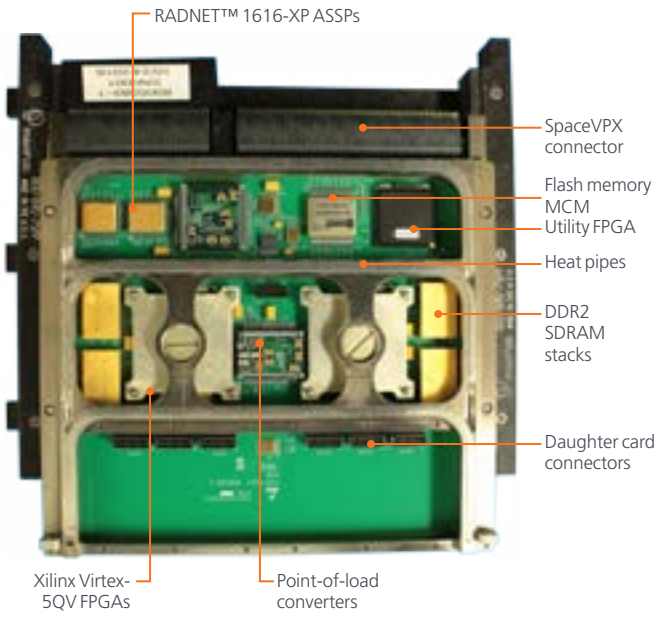
SpaceVPX Reconfigurable Computing Module

The **SpaceVPX Reconfigurable Computing Module** (RCM) fills the gap between computing engines and custom, application-specific integrated circuit-based functions.

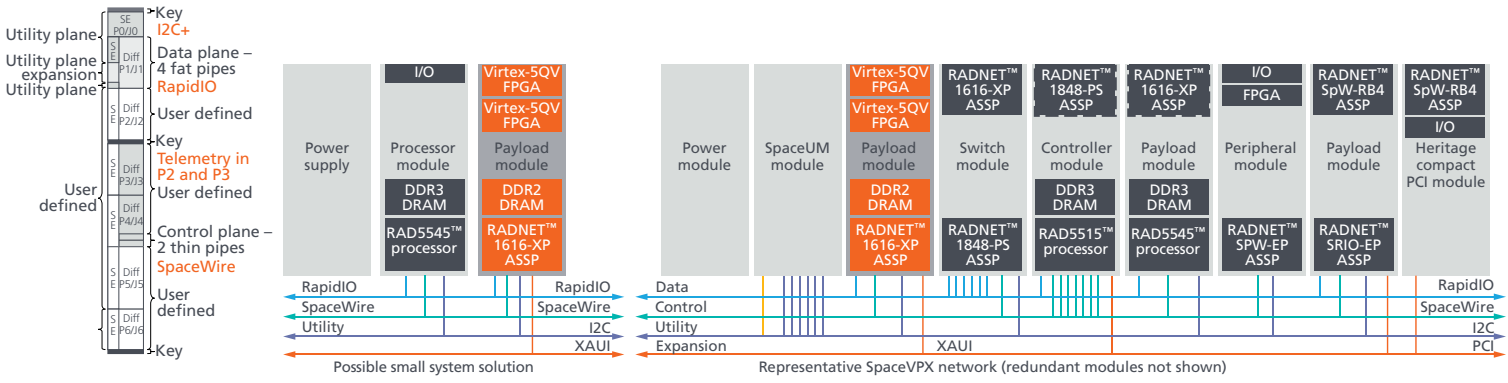
The signal processing logic can convert, decimate, filter, or measure high-speed data from input sources prior to using storage devices or general-purpose processors. The RCM can also transport, expand, encode, or generate high-speed data taken from storage or received from processing engines. This is all completed using high-performance, reconfigurable logic fabric.

The RCM integrates two radiation-hardened Xilinx® Virtex®-5QV field-programmable gate arrays (FPGAs) with SDRAM and flash memory as well as a pair of RADNET™ 1616-XP crosspoint switches on a 6U-220 format module compliant to the ANSI/VITA 78.00 SpaceVPX standard.

The RCM is designed to operate as a payload module in a SpaceVPX backplane. Through the utility FPGA, the RCM provides a primary/redundant SpaceWire link at 100 Mbits/second to the backplane. The crosspoint switches provide protocol agnostic primary/redundant switching to the four serializer/deserializer (SERDES) "fat pipe" backplane ports.



Hardware block diagram



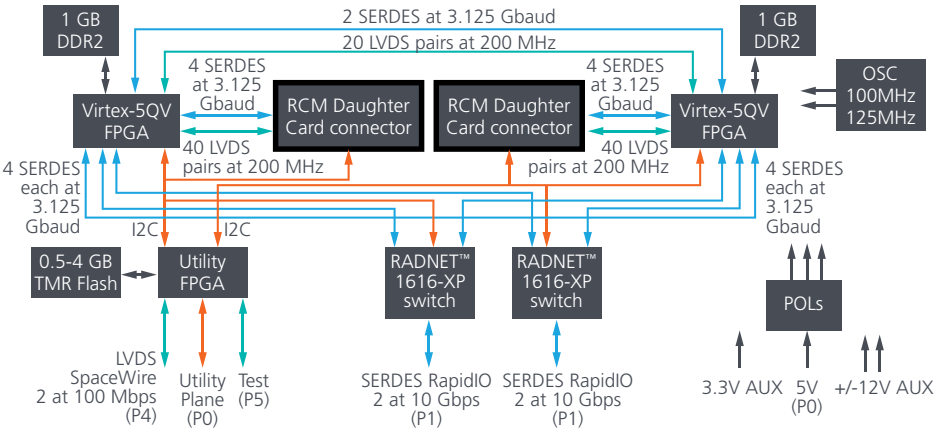
Key features and benefits

- Direct connections between the two FPGAs are provided through six lanes of SERDES and 20 low voltage differential signaling pairs, providing significant flexibility for user-specific applications and data processing
- Dedicated daughter card interfaces associated with each FPGA support mission-specific interfaces and functionality
- The two daughter card slots may use different daughter cards for each FPGA for flexibility or may optionally be combined into a single card supporting both FPGAs for area efficiency
- Included with the RCM is user-configurable FPGA gateware for an FPGA infrastructure core that provides compatibility with the SpaceVPX standard connections to the hardwired module interfaces and additional functionality to decrease the cost and risk of designs. (Note: infrastructure core incorporates Xilinx LogiCORE IP, which must be licensed separately from Xilinx)
- Designed for insertion into the SpaceVPX backplane to support the SpaceWire control plane and system management inter-integrated circuit utility plane for interoperability with other SpaceVPX-compliant boards
- Triple modular redundant flash memory enables high-density non-volatile storage with high reliability
- Each Xilinx FPGA includes two memory ports of 512 MB (64 bits + ECC) DDR2 SDRAM each to provide on-card storage

Specifications

SpaceVPX	**Slot profiles:** **Payload:** SLT6-PAY-4F2T-10.2.1
	Module profiles: **Payload:** MOD6-PAY-4F2T-12.2.1-4-22
	Mechanical size: 6U-220
	Card pitch: 1.2 inches
	Cooling: conduction
	Power profile: +/- 12.0 V (+/- 10%): daughter card dependent 5.0 V (+/- 10%): daughter card dependent 3.3 V AUX: <1.0 Amps
	User-defined I/O: differential
Temperature	Operating at -55 to +125 degrees Celsius
Radiation-hardness	Total ionizing dose: 100 Krad (Si)
	Latchup immune
Power	Highly application dependent. 40-45 Watts for a typical FPGA instantiation with wedgelock interface at 71 degrees Celsius and all dissipation interfaces operational
Interfaces	Up to four (or two dual redundant) four-lane RapidIO ports at up to 3.125 Gbaud per lane with primary/redundant switching to the backplane
	Up to six SERDES lanes between the FPGAs
	Up to 20 LVDS pairs at up to 200 MHz between the FPGAs
	Single (primary/redundant) SpaceWire serial link to the backplane up to 100 Mb/s
	16 discretes between utility FPGA and each Virtex-5QV FPGA
	I2C and related utility plane control signals
	JTAG test and debug
Daughter card Interfaces	Four SERDES lanes at up to 3.125 Gbaud/lane
	40 LVDS pairs at up to 200 MHz

Hardware block diagram



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