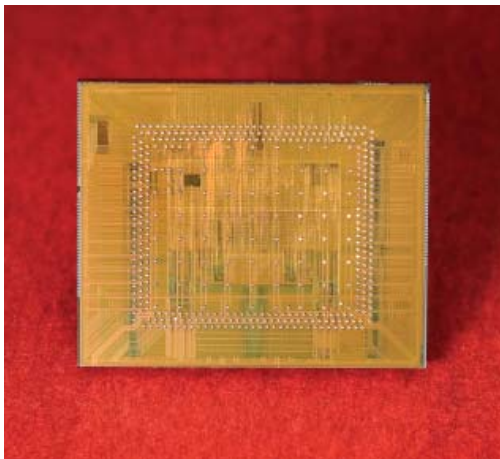


SpaceWire radiation-hardened ASIC

FEATURES AND CAPABILITIES

BAE Systems' SpaceWire is a fully ECSS-E-50-12A-compliant, application-specific integrated circuit that incorporates quad SpaceWire, high-speed, point-to-point LVDS interfaces, a SpaceWire router, and dual PCI 2.0-compliant bus ports.

It supports data rates up to 260 MHz per link. The integrated LVDS I/O are cold-spliceable, ESD-protected, and do not require the use of external LVDS drivers and receivers. The interconnected SpaceWire links and router form a spacecraft network.



SpaceWire ASIC also can be used as a stand-alone link. It implements the SpaceWire reliable transport layer and includes an embedded microcontroller to enable hardware delivery and software-based management support, including the cyclic redundancy check CRC generation and header append and strip mechanism. The SpaceWire ASIC design significantly leverages the BAE Systems Power PCI Bridge design.

This product comes with a C compiler for the embedded microcontroller (EMC). The EMC is a programmable processor that can be used for monitoring and controlling all the functional cores in the ASIC.

The SpaceWire ASIC operates over the full military temperature range and requires a $3.3V \pm 10\%$ I/O and $2.5V \pm 10\%$ core voltage.

BAE Systems' enhanced bulk complementary metal-oxide semiconductor technology is radiation-hardened through the use of advanced proprietary design, layout, and process hardening techniques. The SpaceWire ASIC is fabricated with BAE Systems' space-qualified R25 radiation-hardened technology, and is designed for use in systems operating in radiation environments.

The BAE Systems SpaceWire ASIC development was sponsored by NASA's Glenn Research Center and Goddard Space Flight Center, including the joint-ASIC development with NASA Goddard.

Standard microcircuit drawing #5962R08A04

QML-compliant part

SpaceWire interface

- 260 MHz
- Compliant-standard four ports

Memory interface

- Electrically erasable, programmable, read-only memory for initialization
- Memory storage: synchronous dynamic random-access memory or static random-access memory

Dual-user PCI ports

- Up to 33 MHz operation
- 32 bit address/data bus

Test interfaces

- 16550 UART
- JTAG
- Non-invasive SpaceWire data access

Operating temperature range -55°C to 125°C

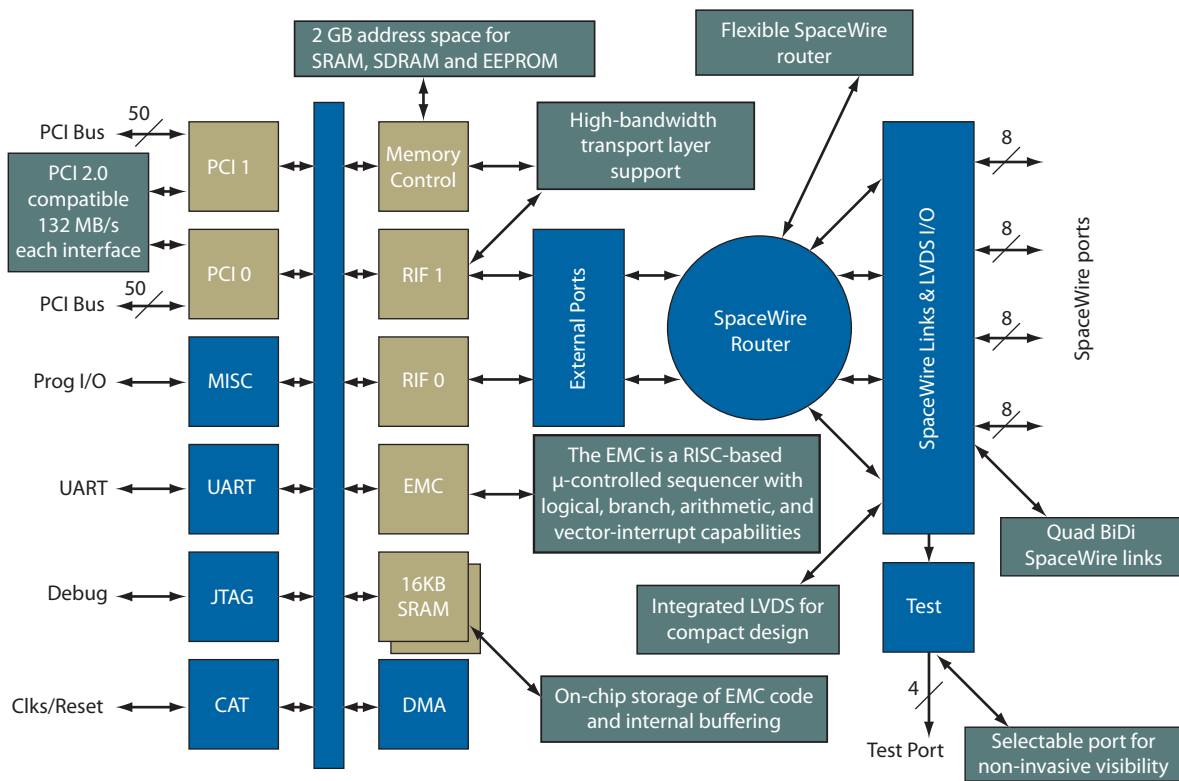
Packaging

- TRL-9-qualified, 32 mm ceramic column grid array

Radiation levels

- Total ionizing dose $< 2 \times 10^5$ rad (Si)
- Single-event upset $< 1 \times 10^9$ upsets/bit day
- Latchup-immune

SPACEWIRE ASIC FUNCTIONAL BLOCK DIAGRAM



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