

MILLENNIUM 4Mb Radiation-Hardened SRAM

The MILLENNIUM SRAM is our next generation high speed memory product for users in the space community. Capable of withstanding the effects of natural space, MILLENNIUM has total dose tolerance of greater than 200 Krads and an upset rate of less than 1E-10 upsets per bit-day. Prompt dose levels are >1E9 rad/sec. Flight hardware being delivered now.

MILLENNIUM FAMILY OF PRODUCTS

4 Mb single chip, up to 20 Mb multi-chip modules available

512K × 8 SRAM

- 40 lead flatpack
- 36 lead flatpack

512K × 32 SRAM

- 84 lead flatpack

512K × 40 SRAM

- 84 lead flatpack

1M × 8 and 2M × 8 configurations available

FEATURES AND CAPABILITIES

Read/write access times of 15-17 ns

Operation from -55°C to +125°C

Supply voltage of 2.5V

I/O voltage of 2.5V or 3.3V

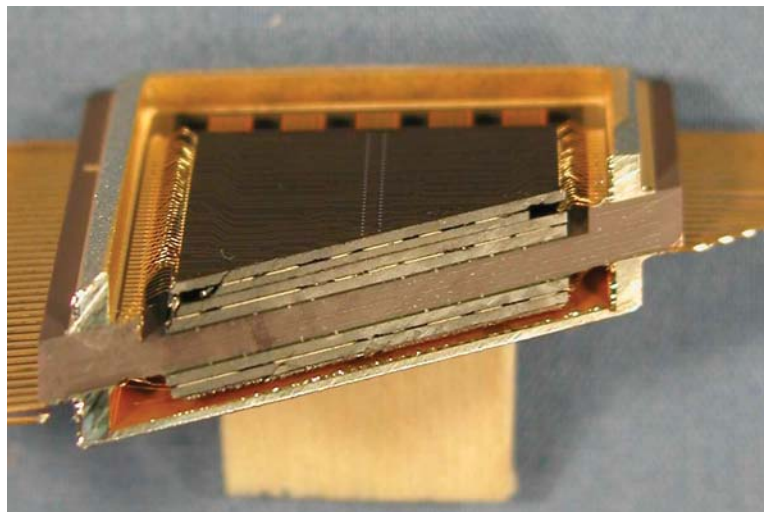
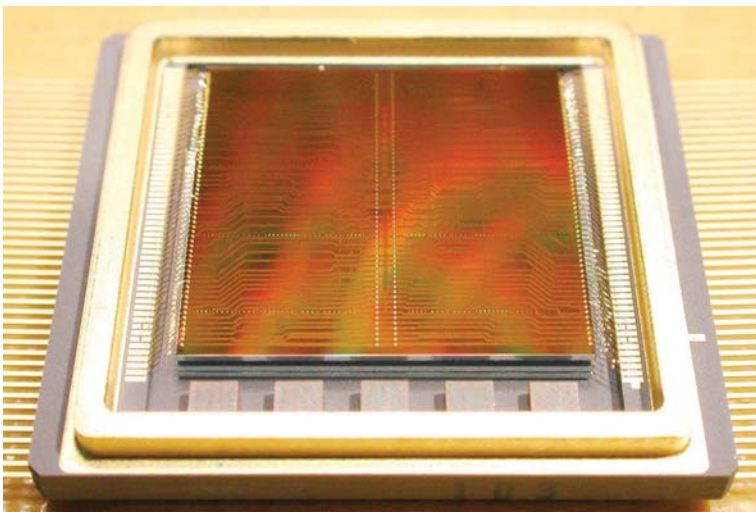
Standby current 20-50 mA

Asynchronous operation

Prototype and flight flows

Latch-up immune

Operating power < 13 mW per MHz



SYSTEM DEFINITIONS

A:0-18 Address input pins that select a particular eight-bit word within the memory array.

DQ:0-7 Bi-directional data pins that serve as data outputs during a read operation and as data inputs during a write operation.

\bar{S} Negative chip select, when at a low level, allows normal read or write operation. When at a high level, \bar{S} forces the SRAM to a precharge condition, holds the data output drivers in a high impedance state and disables the data input buffers only. If this signal is not used, it must be connected to GND.

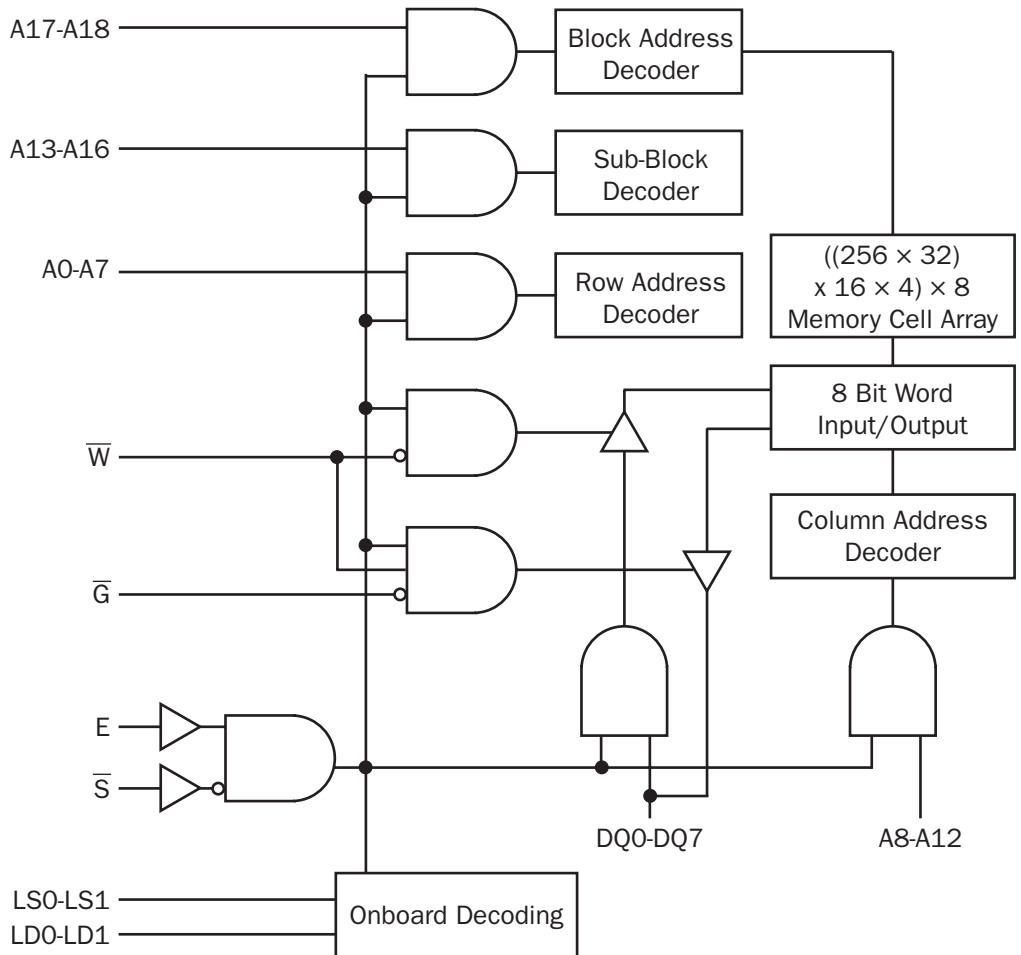
LS/LD LS0, LS1 selects and LDO, LD1 decode inputs provide externally programmable bank-select decode capability.

\bar{W} Negative write enable, when at a low level, activates a write operation and holds the data output drivers in a high impedance state. When at a high level, \bar{W} allows normal read operation.

\bar{G} Negative output enable, when at a high level holds the data output drivers in a high impedance state. When at a low level, the data output driver state is defined by \bar{S} , \bar{W} , and E. If this signal is not used it must be connected to GND.

E Chip enable, when at a high level allows normal operation. When at a low level, E forces the SRAM to a precharge condition, holds the data output drivers in a high impedance state and disables all the input buffers except the \bar{S} input buffer. If this signal is not used, it must be connected to V_{DD} .

FUNCTIONAL DIAGRAM



FOR MORE INFORMATION, CONTACT:

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